

AN-SL2001-05

Component Selection and Layout Guide for SL2001/ SL2002

Introduction

This document provides component selection, board layout and board metalization guidelines for systems utilizing the SL2001 and SL2002. Two example board layouts are provided to demonstrate the guidelines discussed in this document.

The SL2001 has two different Evaluation Boards available which target 400W and 800W peak power levels and 2 laser types.

SLE2001-E01: 400W peak power capable board with Quad EEL Laser [2].

SLE2001-V01: 800W peak power capable board with VCSEL Laser [3].

The SL2002 has one Evaluation Board available.

SLE2002-R01: 400W peak power capable board with the input voltage range of a single Lithium Ion cell and Resistor (rather than laser) as the load [4].

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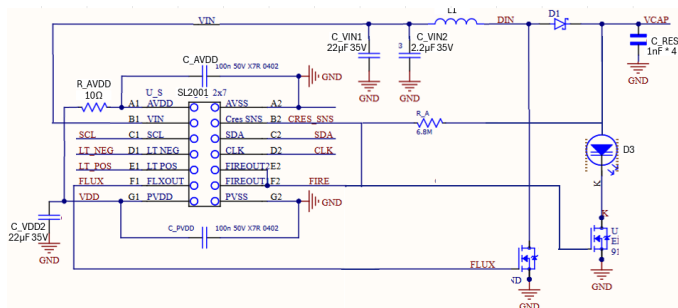
Safety Warning

This device is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing PERMANENT VISION DAMAGE AND BLINDNESS as well as additional injury or property damage. Laser diodes emit light that may be outside of the users' visual range which can cause PERMANENT VISION DAMAGE AND BLINDNESS as well as additional injury or

property damage. Users are fully responsible for following proper laser safety procedures to prevent injury or damage. We recommend the use of Laser Eye Safety Goggles for all testing.

Component Selection and Layout Floorplanning

It is important to select components for a specific floorplan in order to ensure that the board size and form factor will be achieved and that the critical routing will be achievable. The basic schematic showing SL2001/ SL2002 system components needed is shown in Figure 1 below.



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Two floorplan examples are shown in Figures 6 and 11. Please refer to those examples for specific layouts utilizing the recommendations below. When floorplanning, the following guidelines are recommended in order of importance:

1. Laser

Selection: The SL2001/ SL2002 are designed to support a large variety of laser options in order to meet the needs of different applications. Key items to note during the board layout phase include the laser forward voltage and current needed to achieve peak light power as well as the form factor of the laser: (a) packaged or bare die, (b) surface mount or through hole (c) light emitting from the top or one of the sides). For peak power greater than or equal to 400W with pulse widths less than or equal to 3ns, Silanna has found that surface mount packages with anode pins on two sides of a central cathode allow for the most flexibility during board layout; however, the SLE2001-V01 EVB demonstrates that >800W peak power can be achieved using a laser with a single anode pin.

Floorplan: For surface mount lasers, assess whether your thermal plan allows for components to be placed directly under the laser as in the layout floorplan of Figure 6 or on the same board side as the laser as in the layout floorplan of Figure 11. The rest of the floorplanning decisions below will be made with the laser placement in mind.

2. Cres Capacitors

Selection: Silanna recommends using C0G capacitors with as small a footprint as possible for the needed voltage rating. Use as many in parallel as will fit across the footprint of the laser

Floorplan: Place the Cres capacitors such that their positive terminal is as close as possible to the laser anode and their negative terminal will be able to have a very low inductance path to the source of the FireFET.

3. FireFET

Selection: Silanna recommends a GaN FET due to the small footprint and faster turn-on and turn-off than that provided by a silicon FET. For peak power less than 200W and pulse width >20ns, a silicon FET is acceptable.

Floorplan: Place the FireFET such that its drain is as close as possible to the cathode of the laser and its source is close to the negative terminal of the Cres capacitors.

4. SL2001/ SL2002

Selection: SL2001 is targeted for high peak power (>400W) applications and SL2002 is targeted for battery powered applications with lower peak power (typically 200W or less).

Floorplan: Place the SL2001/ SL2002 such that its FireOUT and PVdd pins are as close as possible to the Gate and Source pins of the FireFET.

5. PVdd to PVss Decoupling capacitors

Selection: any type of ceramic capacitor that meets the area, voltage and capacitance needs is acceptable.

Floorplan: Place 1 or 2 0201 sized PVdd to PVss decoupling capacitors (0402 size is OK if you prefer) as close as possible to the PVdd and PVss pins of the SL2001/ SL2002.

6. AVdd to AVss decoupling capacitor

Selection: any type of ceramic capacitor that meets the area, voltage and capacitance needs is acceptable.

Floorplan: Place 1 0201 sized AVdd to AVss decoupling capacitor (0402 size is OK if you prefer) as close as possible to the AVdd and AVss pins of the SL2001/SL2002.

7. Inductor

Selection: Silanna recommends an inductor that provides a good combination of high saturation current, low series resistance and small footprint like the CLT32 series of inductors from TDK.

Floorplan: Place the inductor such that its Vin terminal will be within ~6mm of the Cres capacitors.

8. Vin capacitors

Selection: any type of ceramic capacitance with >22uF value is acceptable. Smaller capacitor values can be

used as long as the capacitance value at the operating voltage is $>6\mu\text{F}$ (noting the voltage coefficient of the capacitor in use).

Floorplan: Place 1 to 4 0603 or 0805 ceramic capacitor(s) with a total capacitance $>22\mu\text{F}$ within 5 mm of the inductor V_{in} terminal. *It is preferred for the inductor V_{in} terminal to be about the same distance from the anodes of lasers that have anode terminals on 2 sides of the central cathode (like the lasers shown in this document).*

9. Schottky Diode(s)

Selection: A Schottky diode is recommended due to fast turn-on and near zero reverse recovery characteristics. In choosing a Schottky diode, ensure that it has adequate breakdown voltage for the maximum voltage on the Cres capacitors and an adequate forward current rating for your peak inductor current. Low series capacitance in the Schottky diode will help reduce power dissipation during charging.

Floorplan: Place 1 or 2 Schottky diodes with their anode(s) close to the switching terminal of the inductor and their cathode(s) close to the laser anode(s).

10. FluxFET

Selection: Silanna boards typically use a GaN FET due to the small footprint that can be achieved for a GaN FET with 100V or higher rating. Silicon FETs would also provide adequate performance for this function.

Floorplan: Place the FluxFET such that its gate is within $\sim 3\text{mm}$ of the SL2001/ SL2002 FluxOUT pin and its drain is close to the inductor switching terminal.

11. Cres SNS resistor(s)

Selection: The Cres_SNS resistor needs to have a voltage rating as high as the Cres capacitors. The KOA SG73P series and Rohm ESR03EZPF series achieve 150V working voltage in an 0603 size (note that most 0402 resistors have a voltage rating of 50V and most 0603 resistors have a voltage rating $<75\text{V}$).

Floorplan: Place the Cres_SNS resistor(s) in remaining available space relatively close to the laser and the SL2001/ SL2002.

12. PVdd Bulk Capacitor

Selection: any type of ceramic capacitor that meets the area, voltage with $>10\mu\text{F}$ of capacitance is acceptable.

Floorplan: Place 1 0603 or 0805 ceramic capacitor with a value of at least $10\mu\text{F}$ close to the PVdd input to your board.

Board metalization Guidelines

Upon completion of the floorplanning, please follow the board metalization guidelines below (arranged in order of importance):

1. Laser Firing Loop: The most important layout consideration in order to achieve a high laser light power peak with a short pulse width is to reduce the parasitic high frequency impedance in the loop made up of the Cres capacitors, Fire FET and laser. Figure 2 highlights this path in the schematic.

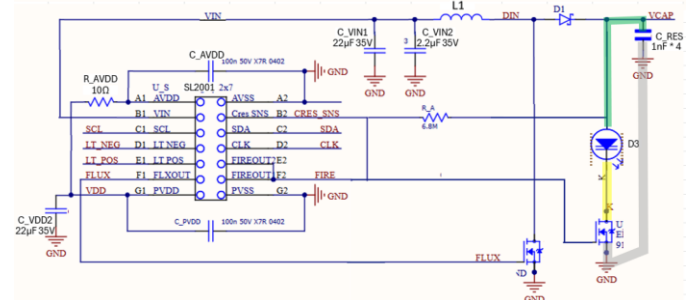


Figure 2: Schematic path for Laser Firing Loop

All of the metal in this loop will see the fast di/dt and high current that will flow through the laser when it is fired. Care needs to be given to ensure that the current carrying capability of the board metal and vias is adequate for the peak and average current specifications of your design. In order to reduce high frequency impedance, the paths should be as direct as possible.

2. FireOUT driving loop: The next most important layout consideration in order to achieve a high laser light peak power with a short pulse width is to reduce the parasitic impedance for the gate driving of the Fire GaN FET. Figure 3 highlights the paths for this loop in the schematic.

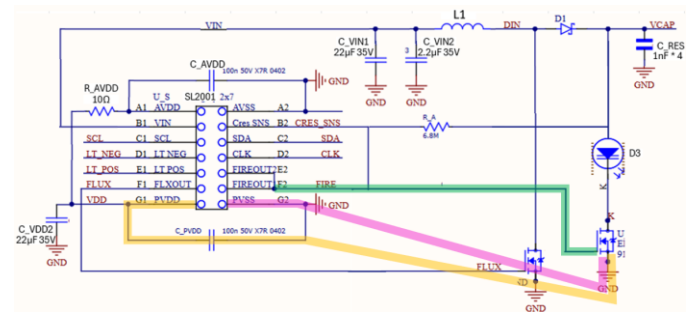


Figure 3: Schematic path for FireOUT driving loop

For FireOUT driving, the FireFET turn-on loop is shown in green and orange in Figure 3 and the FireFET turn-off loop is shown in green and pink in Figure 3. The current in these

loops is much lower than the current through the laser, so the focus of the metalization should be minimization of the inductance.

Note that the orange portion of the FireFET turn-on loop includes the decoupling capacitor. A typical 0402 or 0201 ceramic capacitor has an equivalent series inductance (ESL) of $\sim 350\text{pH}$, so using 2 capacitors in parallel can help reduce the overall loop inductance as long as the routing inductance can be maintained below $\sim 200\text{pH}$.

Note that four terminal capacitors are available with reduced ESL, but the placement of the 4 terminals for positive and negative of those capacitor types do not match well with the PVDD and PVSS pins of the SL2001 and SL2002.

3. Cres Charging Loop: Maintaining a small loop area of the charging loop can reduce the power dissipation of the charger and improve the EMI of the system. Similar to the FireOUT driving loop, Cres charging has two separate paths that both need to be considered for a good board layout. The two separate paths for the Cres charging loop are differentiated by whether the FluxFET is ON (the current through the inductor is ramping up) or OFF (the current through the inductor is charging the Cres capacitors).

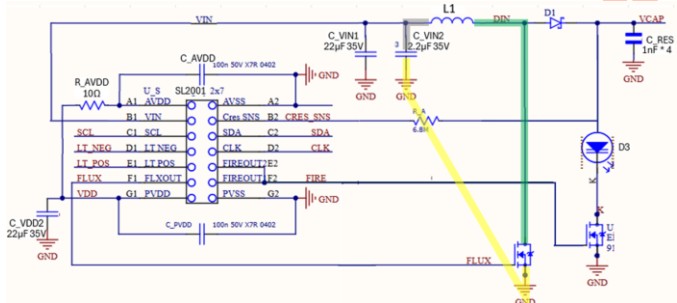


Figure 4: Schematic path for Cres charging with FluxFET ON

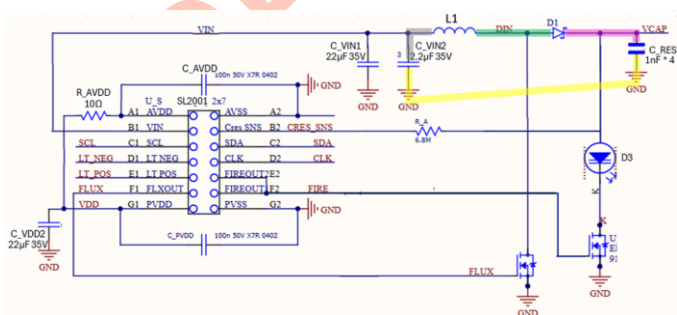


Figure 5: Schematic path for Cres charging with FluxFET OFF

The metal and vias in these paths should be sized for the maximum inductor current. The di/dt in the paths of Figures

4 and 5 is mostly limited by the current change in the inductor, although when the FluxFET is turned off, the ground current for the inductor will change from the source of the FluxFET (yellow path in Figure 4) to the negative terminals of the Cres capacitors (yellow path in Figure 5) very rapidly. So, achieving a low inductance between the source of the FluxFET and the negative terminal of the Cres capacitors is desired.

4. VDD Power and Ground Routing: The SL2001 and SL2002 have separate pins for quiet analog (AVDD and AVSS) and noisy power (PVDD and PVSS) supply and ground. On the IC, there are diodes between PVSS and AVSS and level shifting between the analog and power domains. For best operation, the AVSS and PVSS pins should be via'd down to the ground plane of the board very close to each of those pins.

The PVDD and AVDD domains both are decoupled with $0.1\mu\text{F}$ capacitors to their PVSS and AVSS ground domains as close as possible to the related pins (per the floorplanning recommendations above).

On Silanna evaluation boards, PVDD is the primary VDD supply coming onto the board and AVDD is connected to the PVDD net using a 10Ω resistor. An alternative approach which has worked well for Silanna evaluation is to connect the AVDD domain to the PVDD domain using a PCB trace with an inductance between 10nH and 20nH .

5. CresSNS Resistor: Significant noise reduction circuitry is included for the CresSNS pin on the SL2001 and SL2002, so this resistor can be placed as far as 10mm away from the IC. Please take care to not route noisy signals like CLK, FluxOUT or FireOUT directly adjacent to the Cres route.

6. CLK routing: The CLK input on the SL2001/ SL2002 has hysteresis and noise mitigation circuitry. It is recommended to terminate this signal to the AVSS ground domain of the SL2001/ SL2002 using a 50Ω resistor.

7. SDA/SCL routing: The SDA and SCL inputs on the SL2001/ SL2002 have hysteresis and noise mitigation circuitry. It is recommended to terminate both signals to the AVDD domain of the SL2001/ SL2002 using a $1\text{k}\Omega$ resistor.

SLE2002-R01 Example Board Layout

In the 3D view of the SLE2002-R01 board from [Figure](#) ,

- the laser is placed on the top side of the board
- the Fire GaN FET and Cres capacitors are placed directly under the laser on the bottom side of the board

For this style of component placement, it is important to use a relatively thin board thickness (200um to 600um board thickness is recommended).

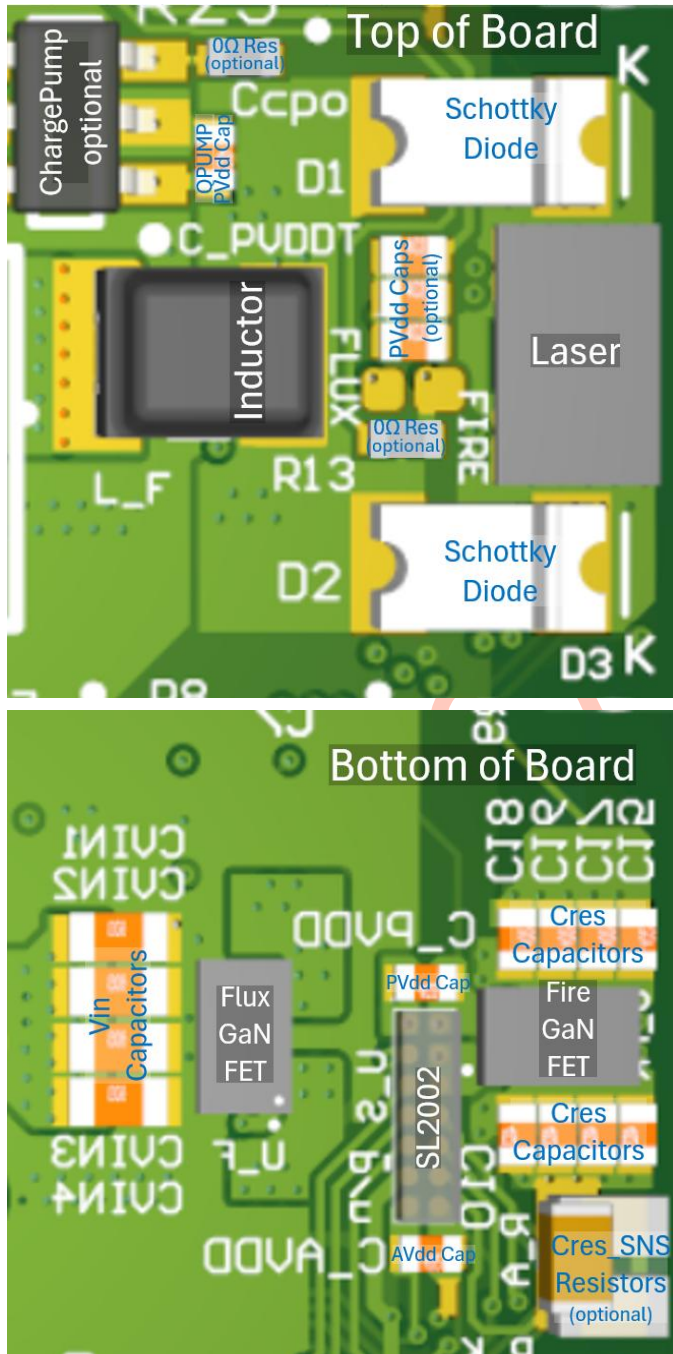


Figure 6: 3D view of SLE2002-R01 laser loop section

1. Laser firing loop: In [Figure](#) below, note the key paths marked in yellow (path from Fire GaN FET drain to cathode of laser), green (path from negative terminal of Cres capacitors to source of Fire GaN FET) and white (path from the positive terminal of the Cres capacitors to the anode of the laser).

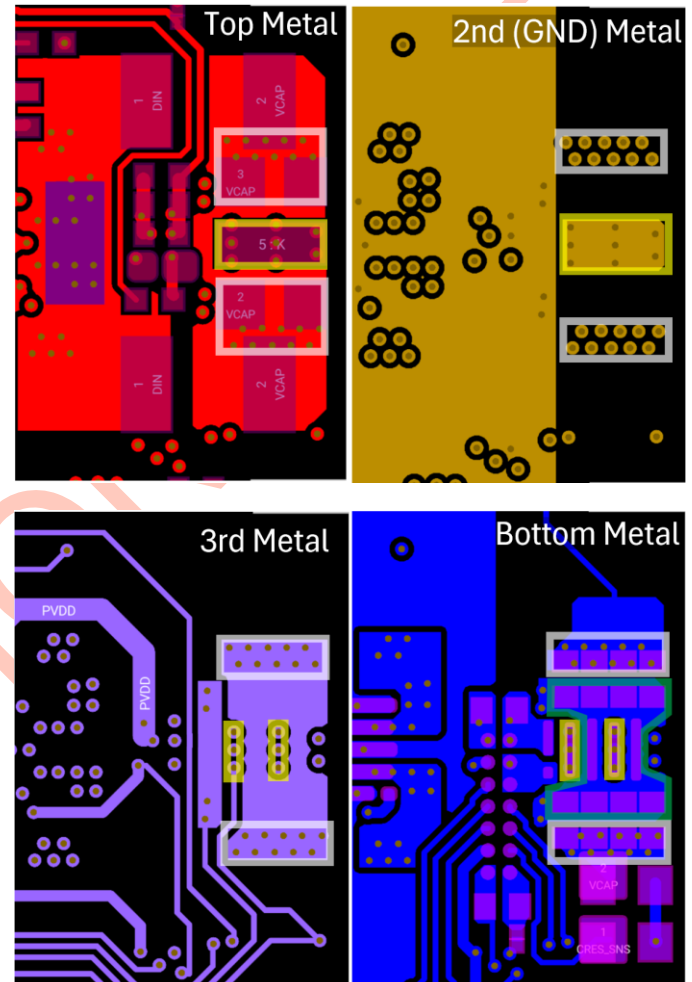


Figure 7: Layout Drawings of SLE2002-R01 laser loop section

Laser cathode to FET drain: The yellow path is directly down from the cathode of the laser on the top of the board to the drain fingers of the Fire GaN FET on the bottom of the board.

FET source to Cres: The green path is completely on the bottom of the board from the Cres capacitor negative terminals to the source fingers of the Fire FET.

Cres to Laser Anode: The white path is almost directly down from the laser anode pads on the top of the board to the top terminal of the Cres capacitors on the bottom of the board. Since the EEL laser shown in this Figure has anode pads above and below the central cathode pad, almost all of the current will flow from the Cres capacitors on top of

the cathode to the top anode pads or from the Cres capacitors below the cathode to the bottom anode pads. The Cres net connection on the 3rd metal layer from the top anode pads to the bottom anode pads is only needed for lower frequency balancing of the Cres capacitor voltage.

2. FireOUT driving loop: Figure highlights the FireOUT gate driving loops on the same board that were shown in Figure .

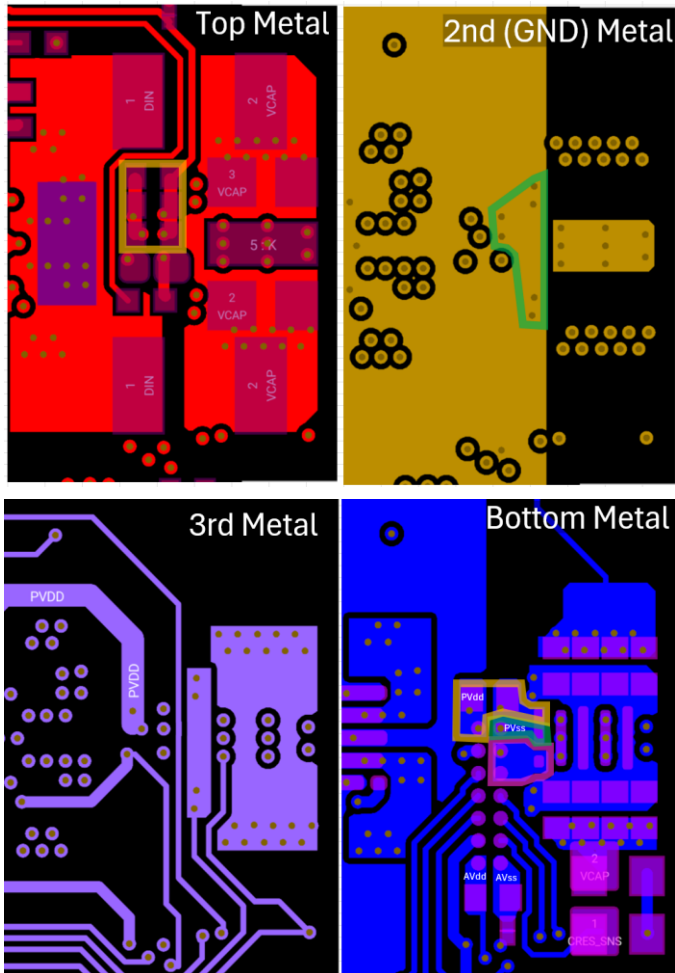


Figure 8: Gate Path from SL2002 Fireout pins to FireFet

In Figure above, note the key paths marked in pink (path from Fire FET gate to FireOUT pins of SL2002), green (path from Fire FET source to the PVSS pin of the SL2002), orange (path from the Fire FET source to the bottom of the PVDD decoupling caps) and orange (path from the FireFET source, through the PVdd decoupling capacitors to the PVDD pin of the SL2002).

FET Gate to SL2002 FireOUT pins: The pink path is completely on the bottom metal layer of the board. Since the SL2002 and the FireFET are both on the bottom side of the board and the size of this loop is small, adding alternate

paths on other board layers would result in very little reduction of the high frequency impedance.

FET Source to SL2002 PVss Pin: The high frequency impedance for this path is critical to the fast turn-off of the FireFET while also helpful to prevent unwanted turn-on of the FireFET. The green path is shared between the bottom layer and the 2nd (GND) metal layer. The portion on the bottom layer provides a low impedance path from the left-most source finger of the FET to the SL2002 PVss pin while the path on the 2nd (GND) layer provides a higher impedance path to the other source fingers of the FET.

FET Source to PVdd capacitor to SL2002 PVdd Pin: The high frequency impedance for this path is critical to the fast turn-on of the FireFET. For the PVdd capacitor on the bottom of the board, almost all of the higher frequency current will flow on the bottom metal layer of the board. The optional additional PVdd capacitors on the top of the board (particularly the capacitor that is directly over the SL2002 PVdd and PVss pins) provide some reduction in the total loop impedance dependent on the thickness of the PCB.

3. Cres charging loop: In Figure 9 below, the key charger loop paths when the FluxFET is on are shown in yellow (capacitor to FluxFET source), white (capacitor to inductor) and green (FluxFET drain to inductor).

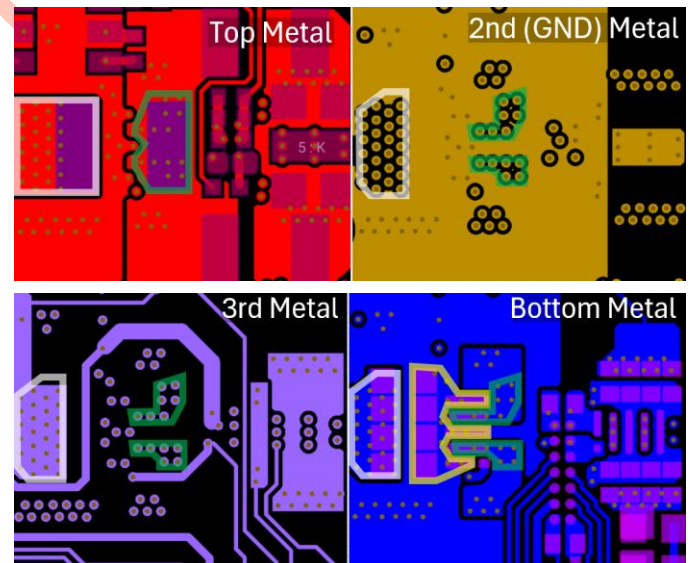


Figure 9: SLE2002-R01 Cres Charge Path – Flux FET ON

Vin cap to FluxFET source: the yellow path is completely on the bottom layer.

Vin cap to inductor: the white path is almost all thru the vias from the Vin capacitors on the bottom of the board to the inductor on the top of the board.

FluxFET drain to inductor: the green path is almost all through the vias from the FluxFET drain on the bottom of the board to the inductor terminal on the top of the board.

In Figure 10 below, the key charger loop paths when the FluxFET is OFF are shown in white (from the Vin capacitors to the inductor), green (from the inductor to the Schottky anodes), pink (from the Schottky cathodes to the Cres capacitors) and yellow (from the Cres capacitors to the Vin capacitors).

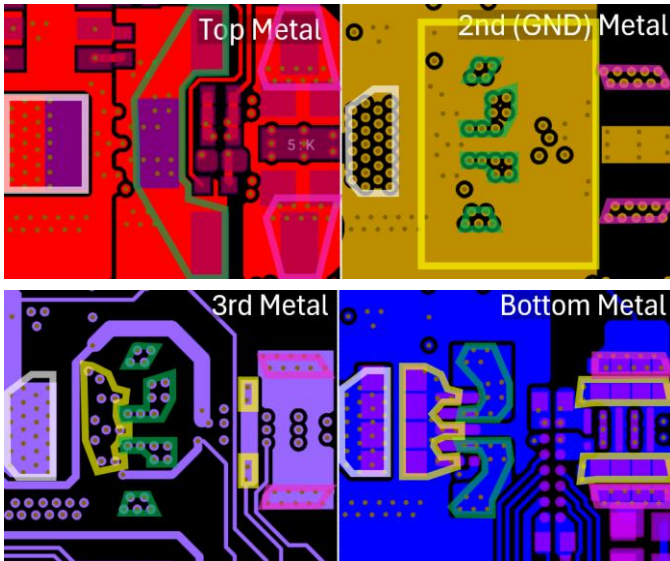


Figure 10: SLE2002-R01 Cres Charge Path – Flux FET OFF

Vin cap to inductor: the white path is almost all thru the vias from the Vin capacitors on the bottom of the board to the inductor on the top of the board.

Inductor to Schottky anodes: the green path current flows almost entirely on the top metal layer. The shapes on the bottom metal layer are primarily present to decrease the impedance from the FluxFET drain to the Schottky anodes as that path can see high di/dt 's if the Vres net falls below ground during laser firing.

Schottky cathodes to Cres caps: the pink path has some impedance on the top layer with most of the impedance through the vias from the top layer down to the Cres capacitors on the bottom of the board.

Cres caps to Vin caps: the yellow path starts along the bottom metal layer from the Cres capacitors, then travels through 2 vias on the left side of each capacitor bank up to the 2nd (GND) metal layer. It continues along the 2nd (GND) metal layer to a group of vias next to the Vin capacitor bank negative (GND) terminals. It travels through those vias down to the Vin Capacitors on the bottom of the board.

4. VDD Power and Ground Routing: In Figure 8, the SL2002 PVss pin is connected to the ground plane with a via directly under its bump, while the SL2002 AVss pin is connected to the ground plane 1.6mm away from its bump in order to stay out of the direct current path between the PVss pin of the board and the ground terminals of the Cres capacitors. The AVdd net is connected to the PVdd net through a 10Ω resistor near to the PVdd pin of the board.

Metal Core Example Board Layout

Next, an example board is shown with only 2 routing layers and components all on the top of the board. This board required more floorplan work, and was unable to achieve the loop inductance of more complex boards, but was able to achieve the key goals described in this document with superior performance to other boards using similar constraints.

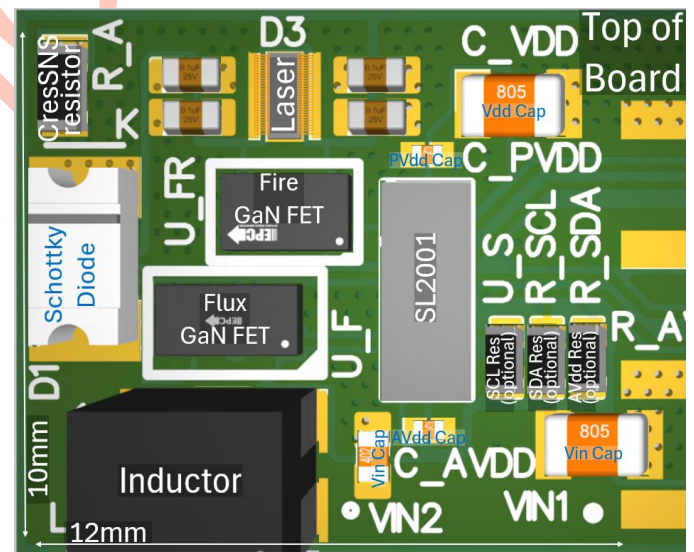


Figure 11: 3D view for a board with components on top only

1. Laser firing loop: In Figure 12 below, note the key paths marked in yellow (path from Fire FET drain to cathode of laser), green (path from negative terminal of Cres capacitors to source of Fire FET) and white (path from the positive terminal of the Cres capacitors to the anode of the laser).

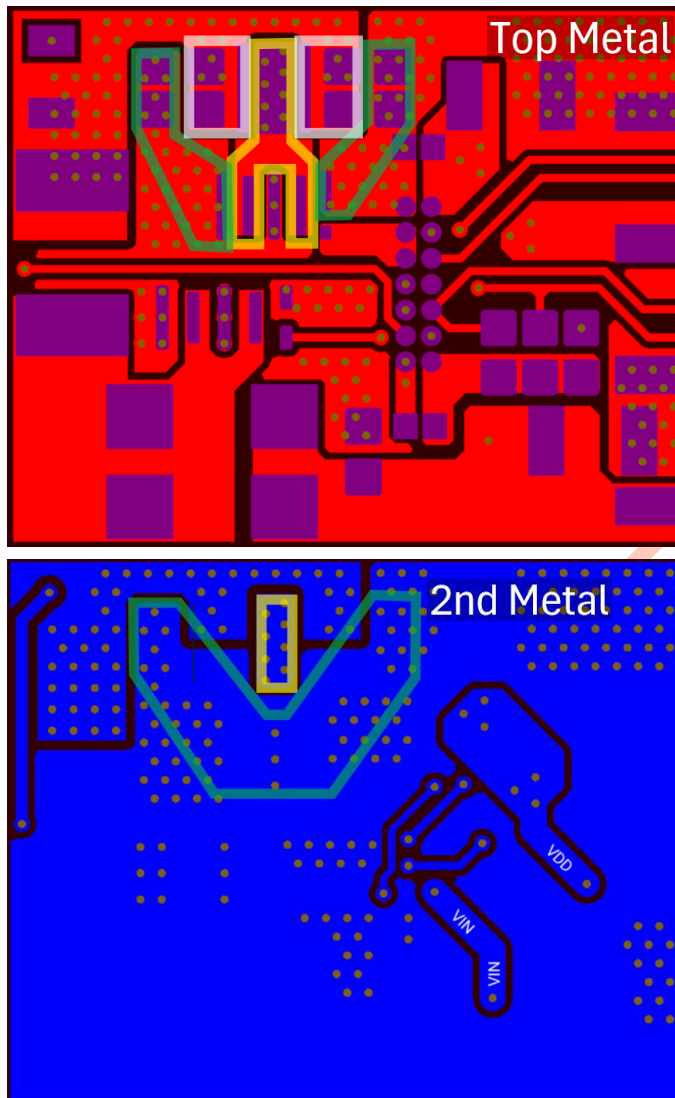


Figure 12: Top and second metal layout drawing for a board with components on top only

Laser cathode to FET drain: In *Figure*, the yellow path is almost all along the top metal layer with the Fire GaN and laser cathode placed as close as possible to each other. The vias under the laser cathode are purely for thermal conduction as this board has a metal core under the 2 board layers.

FET source to Cres: In *Figure*, the green (GND) path is in parallel along the top metal layer and the 2nd metal layer.

The middle source finger of the Fire FET has almost all current flow on the 2nd metal layer.

Cres to Laser Anode: In *Figure*, the white path is almost entirely on the top layer with the laser anode and Cres capacitor top terminals placed very close to each other. As discussed in the Cres Charging Loop section, the anodes on the right and left side of the laser are shorted, but that is only needed for charging of the Cres capacitors from the Schottky diode and for lower frequency balancing of the left and right side Cres capacitors.

2. FireOUT driving loop: *Figure* shows the metal core board layout of this 2nd most critical loop. Note that the key paths marked in pink (path from Fire FET gate to FireOUT pins of SL2001), green (path from Fire FET source to the SL2001 PVSS pin) and orange (path from the FireFET source, through the PVdd decoupling capacitors to the PVDD pin of the SL2002).

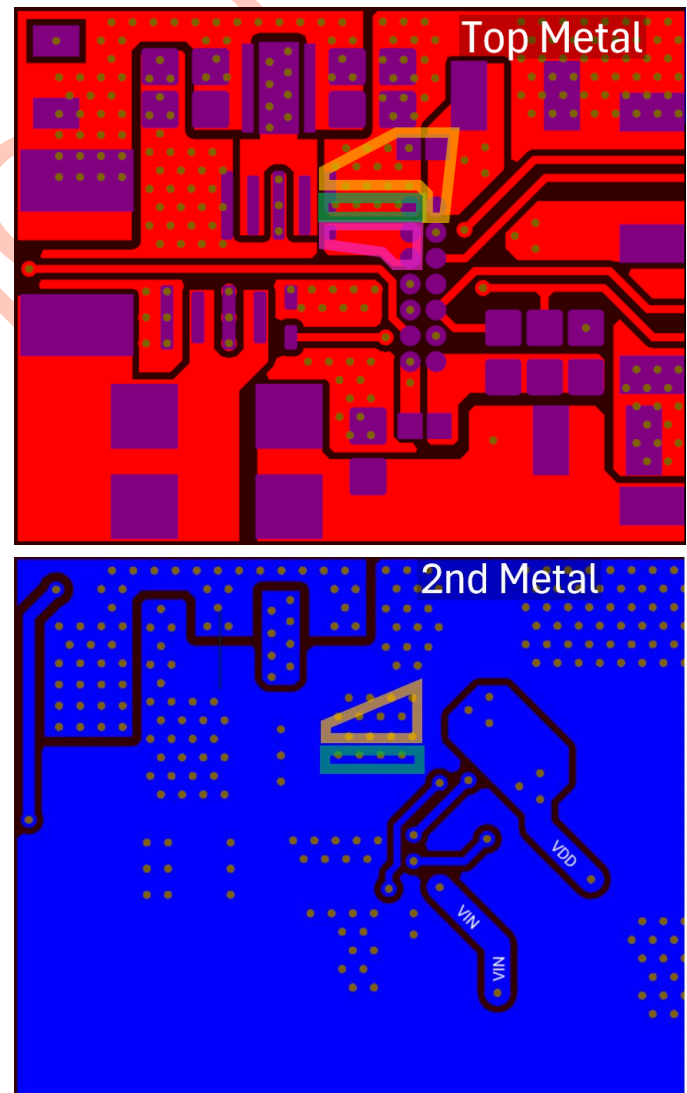


Figure 13: Fire FET Gate path to Fireout pins of SL2001

FET Gate to SL2001 FireOUT pins: The pink path is completely on the top metal layer of the board. Since the SL2001 and the FireFET are both on the top side of the board and the size of this loop is small, adding alternate paths on other board layers would result in very little reduction of the high frequency impedance.

FET Source to SL2001 PVss Pin: The high frequency impedance for this path is critical to the fast turn-off of the FireFET while also helpful to prevent unwanted turn-on of the FireFET. The green path is shared between the top layer and the 2nd (GND) metal layer. Most of the high frequency current flows on the top layer, but the 2nd (GND) layer helps to spread the source current to the other source fingers.

FET Source to PVdd capacitor to SL2001 PVdd Pin: The high frequency impedance for this path is critical to the fast turn-on of the FireFET. For the PVdd capacitor closest to the SL2001, almost all of the high frequency current will flow on the top metal layer. Ground current for the additional 0805 PVdd capacitor further away from the SL2001 and FireFET will flow mostly along the 2nd (GND) layer.

3. Cres charging loops: In Figure 14 below, the key charger loop paths when the FluxFET is on are shown in yellow (capacitor to FluxFET source), white (capacitor to inductor) and green (FluxFET drain to inductor).

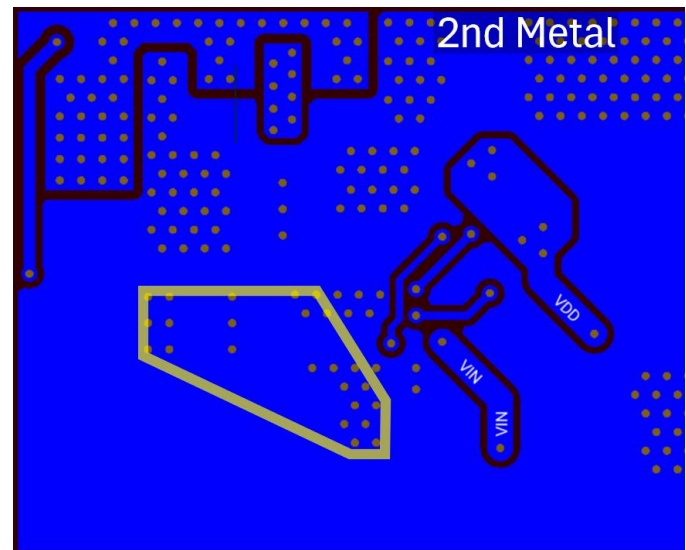
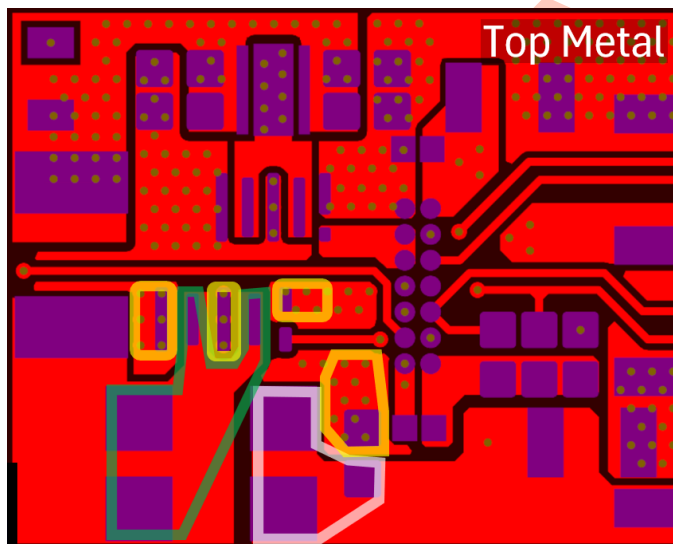


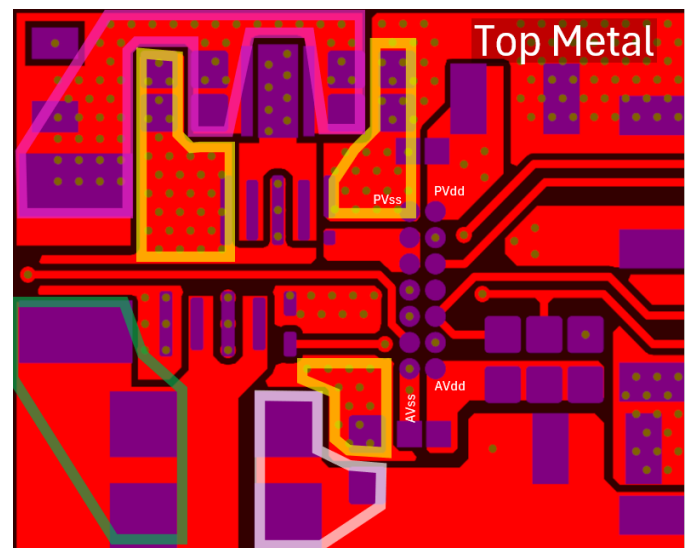
Figure 14: Metal Core Cres Charge Path – Flux FET ON

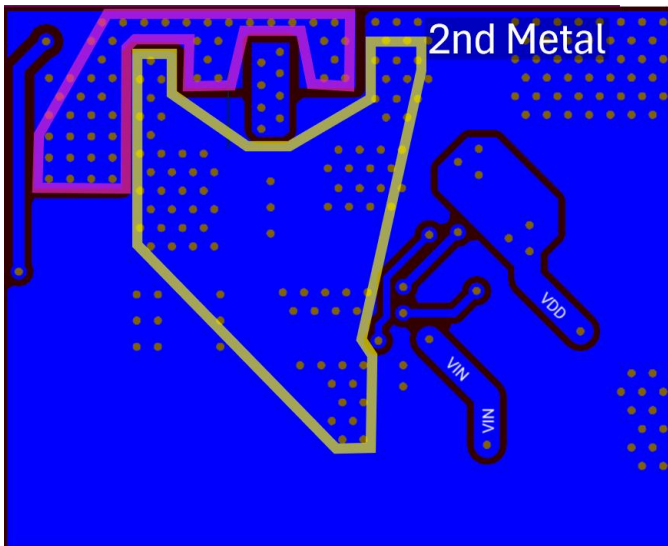
Vin cap to FluxFET source: the yellow path is shared between the top and 2nd (GND) layers. It is important to maintain a continuous 2nd (GND) layer path.

Vin cap to inductor: the white path is entirely on the top metal layer.

FluxFET drain to inductor: the green path is also entirely on the top metal layer.

In Figure 15 below, the key charger loop paths when the FluxFET is OFF are shown in white (from the Vin capacitors to the inductor), green (from the inductor to the Schottky anode), pink (from the Schottky cathodes to the Cres capacitors) and yellow (from the Cres capacitors to the Vin capacitors).





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Vin cap to inductor: the white path is entirely on the top metal layer.

Inductor to Schottky anodes: the green path current flows entirely on the top metal layer since the 2 terminals are very close to each other.

Schottky cathodes to Cres caps: the pink path shares impedance between the 2 metal layers of this board. The impedance is relatively high and not balanced well between the left and right sides of the laser. This imbalance can be mitigated by waiting >200ns after charging the Cres capacitors before firing the laser (via the programmable charge time of the SL2001/ SL2002) and by not allowing the Cres voltage to fall more than 5V below ground during laser firing.

Cres caps to Vin caps: the yellow path is travels mostly on the 2nd (GND) metal layer with care taken to maintain a

continuous 2nd (GND) layer path. Many vias are placed in the terminations of the top metal layer for the Cres capacitors and the Vin capacitors.

4. VDD Power and Ground Routing: In Figure 15, the SL2001 PVss and AVss bumps have vias to the ground plane very close to their bumps. The top metal layer is broken in between the AVss vias and the GND vias of the Vin decoupling capacitor in order to reduce the Vin switching noise see on the AVss bump. The AVdd net is connected to the PVdd net through a 10Ω resistor to the right of the SL2001.

Summary and Conclusions

SL2001 and SL2002 parts provide a flexible Laser Firing solution, but the achievable peak laser power, pulse width and board power dissipation require careful component selection and board layout techniques. This document has provided guidelines and two example board layouts that can help achieve very high performance in the system. For more details, such as experimental results, please refer to the Datasheets and Evaluation Board Application Notes in the Reference section below or contact Silanna's Marketing Application team.

References

- [1] Datasheet for SL2001 & SL2002
- [2] SL2001 400W EEL Application Note
- [3] SL2001 800W VCSEL Application Note
- [4] SL2002 400W resistive load Application Note

Revision History

Revision	Date	Author	Note
0.1	4 Apr 2025	AZ	Draft release.
1.0	16 Oct 2025	BR/AZ	Document Control Upload