## SD2142ET OVERVIEW

The SD2142ET is a dual-channel, 12-bit, analog-to-digital converter (ADC) supporting sampling rates up to 65MSps. The SD2142ET supports an extended temperature range of -55°C to 125°C. The device uses a multistage pipeline architecture to achieve high signal-to-noise ratio (SNR) and linearity, over wide input signal bandwidth. The SD2142ET can be set to operate using either CMOS or LVDS output interface. Programming for configuration and control is accomplished using a 4-wire SPI-compatible serial bus. The digital output data can be programmed to be delivered in offset binary, twos complement format, or gray code.

## FEATURES

- Extended temperature range (-55°C to 125°C)
- SNR: 70.5dBFS at $f_{IN}$ = 30.2MHz and $f_S$ = 65MSps
- SFDR: 88.2dBc at $f_{IN}$ = 30.2MHz and $f_S$ = 65MSps
- -146.2dBFS/Hz input-noise at $f_{IN}$ = 30.2MHz and $f_S$ = 65MSps
- 1.8V nominal input
- Typical power consumption: 330mW at 65MSps
- Integer 1-to-8 input clock divider (520MHz maximum input rate)
- Sample rates of up to 65MSps
- 1.8V analog supply voltage
- LVDS (ANSI-644 levels) outputs
- Internal ADC voltage reference
- ADC clock duty cycle correction
- Serial port control
- Energy saving power-down modes

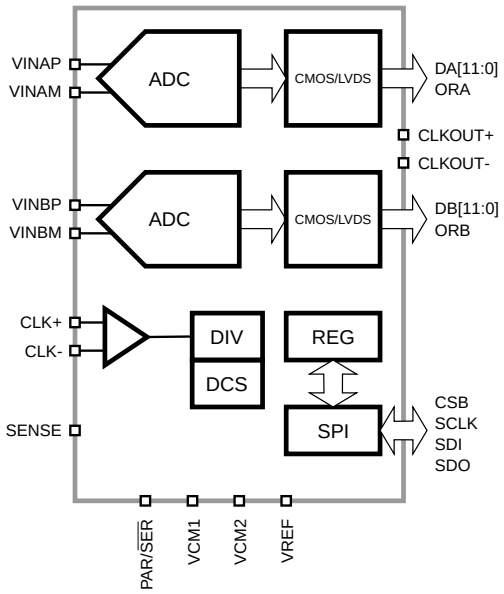


*Figure 1: SD2142ET Functional Block Diagram.*

## APPLICATIONS

- Communications
- General-purpose software radios
- I/Q demodulation systems
- Diversity radio systems
- Smart antenna systems
- Multimode digital receivers
- Ultrasound equipment
- Radar/LiDAR applications

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# SPECIFICATIONS

## DC Specifications

*At $T_A$ = 25°C, $V_{VDD}$ = 1.8V, $V_{OVDD}$ = 1.8V, $F_{CLK}$ = 65MHz, $A_{IN}$ = -1dBFS, differential AC-coupled external clock source, LVDS mode, unless otherwise noted.*

*Table 1. DC Specifications.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 12 | | bits |
| Accuracy | | | | | |
| No Missing Codes | Full | | Guaranteed | | |
| Offset Error | Full | -0.50 | | 0.50 | %FSR |
| Gain Error | Full | -3.00 | | 2.00 | %FSR |
| DNL | Full | | | ±0.5 | LSB |
| INL | Full | | | ±0.8 | LSB |
| Matching | | | | | |
| Offset Error | 25°C | ±-0.80 | | ±0.80 | %FSR |
| Gain Error | 25°C | ±-0.40 | | ±0.40 | %FSR |
| Temperature Drift | | | | | |
| Offset Error | Full | | +/-0.5 | | ppm/°C |
| Gain Error | Full | | 80.0 | | ppm/°C |
| Internal Voltage Reference | | | | | |
| Output Voltage | Full | 1.02 | | 1.07 | V |
| External Voltage Reference | | | | | |
| Range | Full | 0.90 | | 1.07 | V |
| Input Referred Noise | | | | | |
| $V_{REF}$ = 1.0V | 25°C | | 0.40 | | LSB(rms) |
| Analog Input | | | | | |
| Input Span, $V_{REF}$ = 1.0V | Full | | 1.8 | | V |
| Input Capacitance | Full | | 6.0 | | pF |
| Input Resistance | Full | | 2.0 | | kΩ |
| Input Common-Mode Voltage | Full | | 0.70 | | V |
| Input Common-Mode Range | Full | 0.62 | | 0.93 | V |
| VCM Voltage | Full | | 0.67 | | V |
| VCM Current Capability | Full | | 100 | | µA |
| Reference Input Resistance | Full | | 50 | | kΩ |
| Power Supply | | | | | |
| $V_{VDD}$ | Full | 1.7 | 1.8 | 1.9 | V |
| $V_{OVDD}$ | Full | 1.7 | 1.8 | 1.9 | V |
| $I_{VDD}$ @1.8V | Full | | 167 | 215 | mA |
| $I_{OVDD}$ @1.8V (CMOS) | Full | | 12 | 15 | mA |
| $I_{OVDD}$ @1.8V (LVDS) | Full | | 46 | 63 | mA |
| Power Consumption | | | | | |
| Sine Wave Input (CMOS) | Full | | 330 | | mW |
| Sine Wave Input (LVDS) | Full | | 390 | | mW |
| Stand-by[1] | Full | | 60 | | mW |
| Power Down | Full | | 10.0 | | mW |

[1] Stand-by power is measured with a sinewave input and active clock.

## AC Specifications

*At $T_A$ = 25°C, $V_{VDD}$ = 1.8V, $V_{OVDD}$ = 1.8V, $F_{CLK}$ = 65MHz, $A_{IN}$ = -1dBFS, differential AC-coupled external clock source, High-Performance Calibration Mode enabled, background calibration enabled, LVDS mode, unless otherwise noted.*

*Table 2. AC Performance Specifications.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Signal-to-Noise Ratio (SNR) | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | 70.7 | | dBFS |
| $f_{IN}$ = 30.2MHz | 25°C | | 70.5 | | dBFS |
| | Full | 70.5 | | | dBFS |
| $f_{IN}$ = 70.2MHz | 25°C | | 70.3 | | dBFS |
| $f_{IN}$ = 220MHz | 25°C | | 68.2 | | dBFS |
| Signal-to-Noise and Distortion Ratio (SNDR) | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | 70.6 | | dBFS |
| $f_{IN}$ = 30.2MHz | 25°C | | 70.4 | | dBFS |
| | Full | 70.0 | | | dBFS |
| $f_{IN}$ = 70.2MHz | 25°C | | 70.1 | | dBFS |
| $f_{IN}$ = 220MHz | 25°C | | 67.8 | | dBFS |
| Effective Number of Bits (ENOB) | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | 11.4 | | bits |
| $f_{IN}$ = 30.2MHz | 25°C | | 11.4 | | bits |
| $f_{IN}$ = 70.2MHz | 25°C | | 11.4 | | bits |
| $f_{IN}$ = 220MHz | 25°C | | 11.0 | | bits |
| Worst 2nd or 3rd Harmonic Power | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | -89.0 | | dBc |
| $f_{IN}$ = 30.2MHz | 25°C | | -88.2 | -85.0 | dBc |
| $f_{IN}$ = 70.2MHz | 25°C | | -88.2 | | dBc |
| $f_{IN}$ = 220MHz | 25°C | | -81.2 | | dBc |
| Worst Non-Harmonic Power | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | -94.6 | | dBc |
| $f_{IN}$ = 30.2MHz | 25°C | | -94.6 | -84.0 | dBc |
| $f_{IN}$ = 70.2MHz | 25°C | | -94.2 | | dBc |
| $f_{IN}$ = 220MHz | 25°C | | -80.2 | | dBc |
| Spurious-Free Dynamic Range[1] (SFDR) | | | | | |
| $f_{IN}$ = 6.55MHz | 25°C | | 89.0 | | dBc |
| $f_{IN}$ = 30.2MHz | 25°C | | 88.2 | | dBc |
| | Full | 82.0 | | | dBc |
| $f_{IN}$ = 70.2MHz | 25°C | | 88.2 | | dBc |
| $f_{IN}$ = 220MHz | 25°C | | 78.2 | | dBc |
| Two-Tone SFDR | | | | | |
| $f_{IN1}$ = 29.1MHz, $f_{IN2}$ = 30.6MHz | 25°C | | 90.8 | | dBc |
| Crosstalk[2] | 25°C | | -105.0 | | dBc |
| Analog Input Bandwidth | Full | | 650.0 | | MHz |

[1] SNR, SNDR and SFDR exclude the DC and $f_S/2$ bins.

[2] Crosstalk is measured at 100MHz with -1.0dBFS on one channel and no input on the alternate channel.

## Digital Specification

*$V_{VDD}$ = 1.8V, $V_{OVDD}$ = 1.8V, $F_{CLK}$ = 65MHz, $A_{IN}$ = -1dBFS, differential AC-coupled external clock source, DCS disabled, unless otherwise noted.*

*Table 3. Differential Clock Input.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Logic Compliance | Full | | CMOS/LVDS/LVPECL | | |
| Internal Common-Mode Bias | Full | | 0.9 | | V |
| Differential Input Voltage | Full | 0.3 | | 1.2 | $V_{p-p}$ |
| Input Voltage Range | Full | $V_{GND}$-0.3 | | $V_{VDD}$+0.2 | V |
| Input Common-Mode Range | Full | 0.75 | | 1.05 | V |
| High Level Input Current | Full | -10 | | 10 | µA |
| Low Level Input Current | Full | -10 | | 10 | µA |
| Input Capacitance | Full | | 1.7 | | pF |
| Input Resistance | Full | | 6.0 | | kΩ |

*Table 4. CSB, SDI, SCLK in Serial or Parallel Programming Mode SDO in Parallel Programming Mode.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| High Level Input Voltage | Full | 1.22 | | | V |
| Low Level Input Voltage | Full | | | 0.6 | V |
| High Level Input Current | Full | -1 | | 1 | µA |
| Low Level Input Current | Full | -1 | | 1 | µA |
| Input Capacitance | Full | | 1.5 | | pF |
| Input Resistance | Full | | 100 | | kΩ |

*Table 5. SDO (Serial Programming Mode).*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| High Level Output Voltage @50µA | Full | 1.77 | | | V |
| High Level Output Voltage @0.5mA | Full | 1.75 | | | V |
| Low Level Output Voltage @50µA | Full | | | 0.05 | V |
| Low Level Output Voltage @1.6mA | Full | | | 0.10 | V |

*Table 6. CMOS Outputs.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| High Level Output Voltage @50µA | Full | 1.77 | | | V |
| High Level Output Voltage @0.5mA | Full | 1.75 | | | V |
| Low Level Output Voltage @50µA | Full | | | 0.05 | V |
| Low Level Output Voltage @1.6mA | Full | | | 0.10 | V |

*Table 7. LVDS Outputs.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Output Voltage ($V_{OD}$), ANSI Mode | Full | 250 | 300 | 450 | mV |
| Output Offset Voltage ($V_{OS}$), ANSI Mode | Full | 1.10 | 1.13 | 1.30 | V |
| Differential Output Voltage ($V_{OD}$), Reduced Swing | Full | 150 | 220 | 285 | mV |
| Output Offset Voltage ($V_{OS}$), Reduced Swing | Full | 1.10 | 1.22 | 1.30 | V |

## Switching Specifications

*$V_{VDD}$ = 1.8V, $V_{OVDD}$ = 1.8V, $F_{CLK}$ = 65MHz, $A_{IN}$ = -1dBFS, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.*

*Table 8. Clock Input Timing.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Clock Rate | Full | | | 520 | MHz |
| Conversion Rate (after clock divider) | Full | 3.0 | | 65.0 | MHz |
| *CLK Pulse Width High* ($t_{CH}$) | | | | | |
| Divide-by-1 Mode, DCS Enabled | Full | 1.5 | | | ns |
| Divide-by-1 Mode, DCS Disabled | Full | 6.9 | 7.7 | 8.5 | ns |
| Divide-by-2 Mode Through Divide-by-8 Mode | Full | 1.0 | | | ns |
| Aperture Delay ($t_A$) | Full | | 0.5 | | ns |
| Aperture Uncertainty (Jitter, $t_J$) | Full | | 140.0 | | fs |

*Table 9. Data Output.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| *CMOS Mode* | | | | | |
| Data Propagation Delay ($t_{PD}$) | Full | | 6.0 | | ns |
| DCO Propagation Delay ($t_{DCO}$) | Full | | 7.0 | | ns |
| DCO to Data Skew ($t_{SKEW}$) | Full | -1.1 | -0.4 | 0.2 | ns |
| Pipeline Delay (Latency, L) | Full | | 35.0 | | Cycles |
| *LVDS Mode* | | | | | |
| Data Propagation Delay ($t_{PD}$) | Full | | 8.0 | | ns |
| DCO Propagation Delay ($t_{DCO}$) | Full | | 7.7 | | ns |
| DCO to Data Skew ($t_{SKEW}$) | Full | -1.1 | -0.4 | 0.2 | ns |
| Pipeline Delay (Latency, L) Channel A/Channel B | Full | | 32/32.5 | | Cycles |
| Wake-Up Time (from sleep) | Full | | 5.0 | | µs |
| Wake-Up Time (from power down) | Full | | 500.0 | | µs |
| Out-of-Range Recovery Time | Full | | 3 | | Cycles |

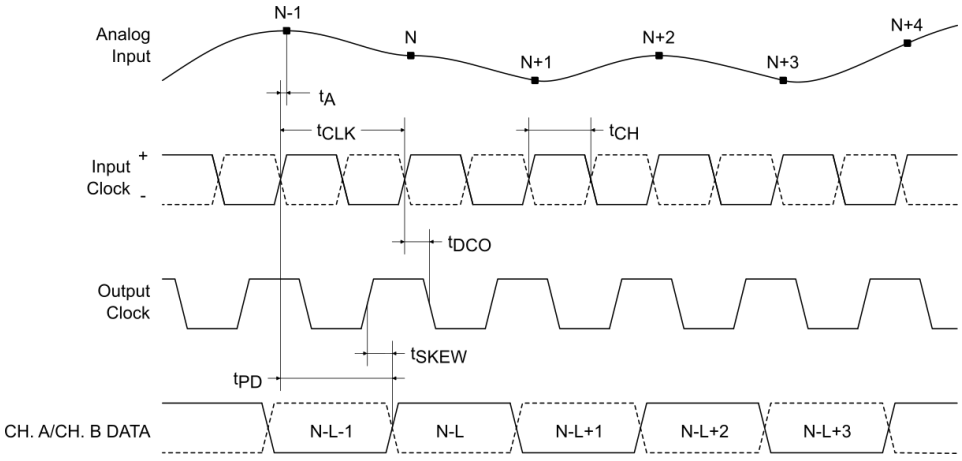



*Figure 2: Parallel CMOS Output Mode Timing.*

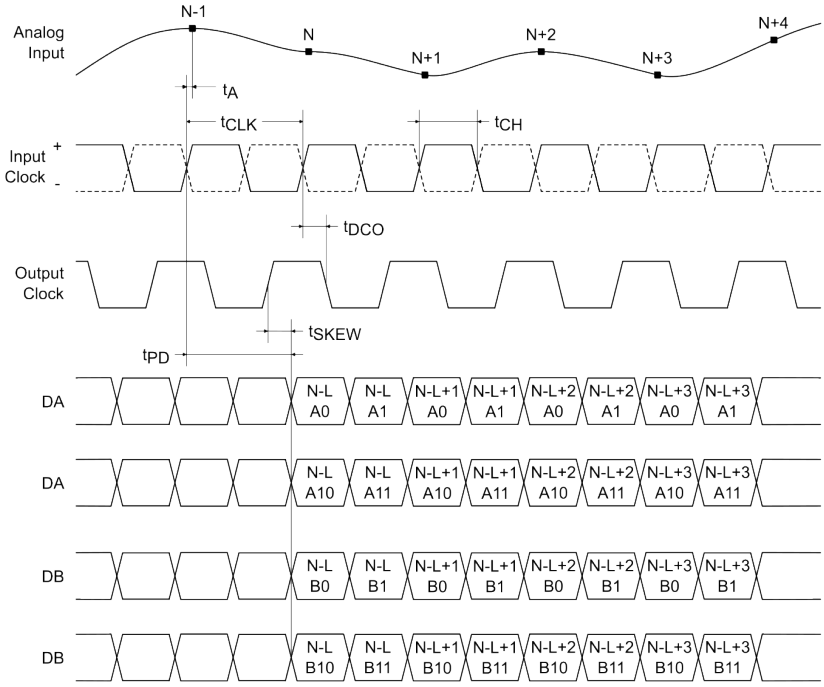



*Figure 3: Channel Multiplexed CMOS Output Mode Timing.*

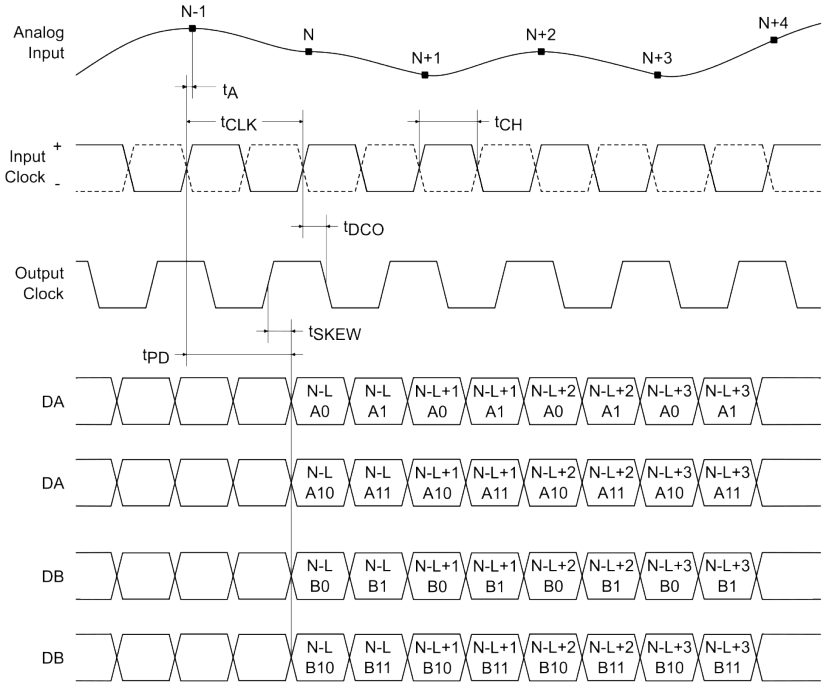



*Figure 4: Channel Multiplexed LVDS Output Mode Timing.*

## Output Modes

The SD2142ET supports both CMOS and LVDS interfaces. Two LVDS samples are sent out every clock cycle using both the rising and the falling edge of the output clock. In interleaved parallel mode, the two ADCs share the full set of output pins. The first half-cycle contains ADC A data and the second ADC B data.

## Output Timing Control

Data delay control, bits [8:5], in register *0x473*, can be used to move the CMOS data relative to output clock. Bit [9] inverts the internal clock sending the data out. Bits [13:10], in register *0x473*, control the output clock delay relative to output data, while bit [14] inverts the clock. The delay step size is about 250ps.

Data delay control is not available in interleaved or multiplexed output mode.

Driving long traces or large load capacitance with CMOS output produces voltage ripple in the digital IO supply and ground, which may couple on chip to the sensitive analog circuits in the ADC and degrade the performance. This effect can be reduced by using an external buffer IC. The use of LVDS output interface largely eliminates issues with IO supply noise.

## ABSOLUTE MAXIMUM RATINGS

*Table 10. Absolute Maximum Ratings ($T_A$ = 25°C, unless otherwise specified).*

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| VDD | $V_{VDD}$ | Relative to GND | -0.3 | 2.0 | V |
| OVDD | $V_{OVDD}$ | Relative to GND | -0.3 | 2.0 | V |
| VINAP/VINBP, VINAM/VINBM | | Relative to GND | -0.3 | 2.0 | V |
| CLK+, CLK- | | Relative to GND | -0.3 | 2.0 | V |
| VCM | | Relative to GND | -0.3 | 2.0 | V |
| VREF | | Relative to GND | -0.3 | 2.0 | V |
| PAR/SER | | Relative to GND | -0.3 | 2.0 | V |
| CSB | | Relative to GND | -0.3 | 2.0 | V |
| SCLK | | Relative to GND | -0.3 | 2.0 | V |
| SDI | | Relative to GND | -0.3 | 2.0 | V |
| SDO | | Relative to GND | -0.3 | 2.0 | V |
| DA0, ..., DA11<br>DB0, ..., DB11 | | Relative to GND | -0.3 | 2.0 | V |
| Operating Temperature Range (Junction) | | | -55 | 125 | °C |
| Maximum Junction Temperature Under Bias | | | | 125 | |
| Storage Temperature Range (Ambient) | | | -65 | 150 | |

Notes:

1. Stresses beyond those listed under Table 10 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The device passed product qualification in accordance with JESD47. Specifically, High-Temperature Operating Life (HTOL), qualification in accordance with JESD22-A108 testing was performed at a junction temperature of $T_j$ = 125°C for 1000 hours across three independent production lots, with sample size of 77 units per lot (231 units total). No failures were observed during full qualification, demonstrating compliance with industry reliability requirements.

**ESD CAUTION**.

**Electrostatic Discharge Sensitive Device.**

Proper ESD precautions should be observed to prevent performance degradation or loss of functionality.

## PACKAGE

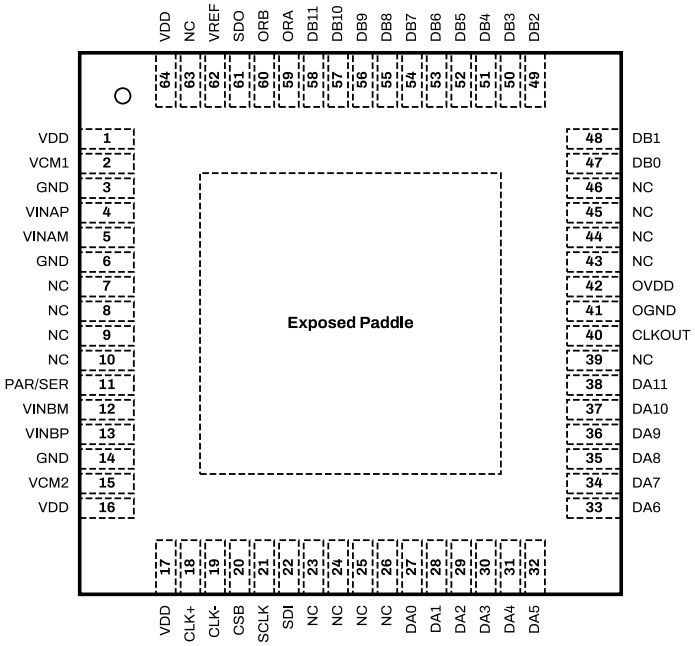



*Figure 5: SD2142ET Package Top View for Parallel CMOS Configuration.*

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

*Table 11. Pin Descriptions for Parallel CMOS Configuration.*

| Number | Name | Type | Comment |
|---|---|---|---|
| 0 | GND | Ground | Exposed Paddle, Analog Ground. |
| 1, 16, 17, 64 | VDD | Power | Analog Supply Voltage. |
| 2 | VCM1 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor. |
| 3, 6, 14 | GND | Ground | ADC Ground. |
| 4 | VINAP | Input | Differential Analog Input Pin (Plus) for Channel A. |
| 5 | VINAM | Input | Differential Analog Input Pin (Minus) for Channel A. |
| 7, 8, 9, 10, 23, 24, 25, 26, 39, 43, 44, 45, 46, 63 | NC | | Do not connect. |
| 11 | PAR/SER | Input | Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCLK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCLK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal. |
| 12 | VINBM | Input | Differential Analog Input Pin (Minus) for Channel B. |

| Number | Name | Type | Comment |
|---|---|---|---|
| 13 | VINBP | Input | Differential Analog Input Pin (Plus) for Channel B. |
| 15 | VCM2 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor. |
| 18 | CLK+ | Input | ADC Clock Input (Plus). |
| 19 | CLK- | Input | ADC Clock Input (Minus). |
| 20 | CSB | Input | SPI Chip Select (Active Low). |
| 21 | SCLK | Input | Serial interface clock input. |
| 22 | SDI | Input | In Serial Programming Mode, (PAR/SER = 0V), SDI Is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part. |
| 27 | DA0 | Output | Channel A CMOS Output Data 0 (LSB). |
| 28 | DA1 | Output | Channel A CMOS Output Data 1. |
| 29 | DA2 | Output | Channel A CMOS Output Data 2. |
| 30 | DA3 | Output | Channel A CMOS Output Data 3. |
| 31 | DA4 | Output | Channel A CMOS Output Data 4. |
| 32 | DA5 | Output | Channel A CMOS Output Data 5. |
| 33 | DA6 | Output | Channel A CMOS Output Data 6. |
| 34 | DA7 | Output | Channel A CMOS Output Data 7. |
| 35 | DA8 | Output | Channel A CMOS Output Data 8. |
| 36 | DA9 | Output | Channel A CMOS Output Data 9. |
| 37 | DA10 | Output | Channel A CMOS Output Data 10. |
| 38 | DA11 | Output | Channel A CMOS Output Data 11. |
| 40 | CLKOUT | Output | Data Output Clock. |
| 41 | OGND | Ground | Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin. |
| 42 | OVDD | Power | Digital I/O Supply. Bypass to ground with a 0.1µF ceramic capacitor. |
| 47 | DB0 | Output | Channel B CMOS Output Data 0 (LSB). |
| 48 | DB1 | Output | Channel B CMOS Output Data 1. |
| 49 | DB2 | Output | Channel B CMOS Output Data 2. |
| 50 | DB3 | Output | Channel B CMOS Output Data 3. |
| 51 | DB4 | Output | Channel B CMOS Output Data 4. |
| 52 | DB5 | Output | Channel B CMOS Output Data 5. |
| 53 | DB6 | Output | Channel B CMOS Output Data 6. |
| 54 | DB7 | Output | Channel B CMOS Output Data 7. |
| 55 | DB8 | Output | Channel B CMOS Output Data 8. |
| 56 | DB9 | Output | Channel B CMOS Output Data 9. |
| 57 | DB10 | Output | Channel B CMOS Output Data 10. |
| 58 | DB11 | Output | Channel B CMOS Output Data 11. |
| 59 | ORA | Output | Channel A Overrange Output. |
| 60 | ORB | Output | Channel B Overrange Output. |
| 61 | SDO | Output | In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part. |
| 62 | VREF | InOut | Voltage Reference Input/Output. |

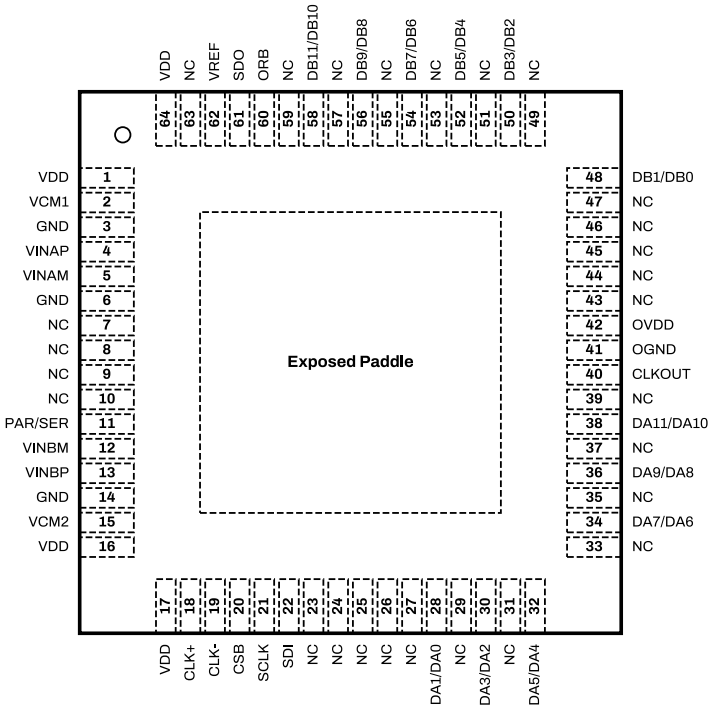



*Figure 6: SD2142ET Package Top View for Channel Multiplexed CMOS Configuration.*

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

*Table 12. Pin Descriptions for Channel Multiplexed CMOS Configuration.*

| Number | Name | Type | Comment |
|---|---|---|---|
| 0 | GND | Ground | Exposed Paddle, Analog Ground. |
| 1, 16, 17, 64 | VDD | Power | Analog Supply Voltage. |
| 2 | VCM1 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor. |
| 3, 6, 14 | GND | Ground | ADC Ground. |
| 4 | VINAP | Input | Differential Analog Input Pin (Plus) for Channel A. |
| 5 | VINAM | Input | Differential Analog Input Pin (Minus) for Channel A. |
| 7, 8, 9, 10, 23, 24, 25, 26, 27, 29, 31, 33, 35, 37, 39, 43, 44, 45, 46, 47, 49, 51, 53, 55, 57, 59, 63 | NC | | Do not connect. |

| Number | Name | Type | Comment |
|---|---|---|---|
| 11 | PAR/SER | Input | Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCLK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCLK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal. |
| 12 | VINBM | Input | Differential Analog Input Pin (Minus) for Channel B. |
| 13 | VINBP | Input | Differential Analog Input Pin (Plus) for Channel B. |
| 15 | VCM2 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor. |
| 18 | CLK+ | Input | ADC Clock Input (Plus). |
| 19 | CLK- | Input | ADC Clock Input (Minus). |
| 20 | CSB | Input | SPI Chip Select (Active Low). |
| 21 | SCLK | Input | Serial interface clock input. |
| 22 | SDI | Input | In Serial Programming Mode, (PAR/SER = 0V), SDI Is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part. |
| 28 | DA1/DA0 | Output | nan |
| 30 | DA3/DA2 | Output | Channel A CMOS Output Data 2 and 3. |
| 32 | DA5/DA4 | Output | Channel A CMOS Output Data 4 and 5. |
| 34 | DA7/DA6 | Output | Channel A CMOS Output Data 6 and 7. |
| 36 | DA9/DA8 | Output | Channel A CMOS Output Data 8 and 9. |
| 38 | DA11/DA10 | Output | Channel A CMOSS Output Data 10 and 11. |
| 40 | CLKOUT | Output | Data Output Clock. |
| 41 | OGND | Ground | Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin. |
| 42 | OVDD | Power | Digital I/O Supply. Bypass to ground with a 0.1µF ceramic capacitor. |
| 48 | DB1/DB0 | Output | Channel B CMOS Output Data 0 and 1. |
| 50 | DB3/DB2 | Output | Channel B CMOS Output Data 2 and 3. |
| 52 | DB5/DB4 | Output | Channel B CMOS Output Data 4 and 5. |
| 54 | DB7/DB6 | Output | Channel B CMOS Output Data 6 and 7. |
| 56 | DB9/DB8 | Output | Channel B CMOS Output Data 8 and 9. |
| 58 | DB11/DB10 | Output | Channel B CMOS Output Data 10 and 11. |
| 60 | ORB | Output | Channel B Overrange Output. |
| 61 | SDO | Output | In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part. |
| 62 | VREF | InOut | Voltage Reference Input/Output. |

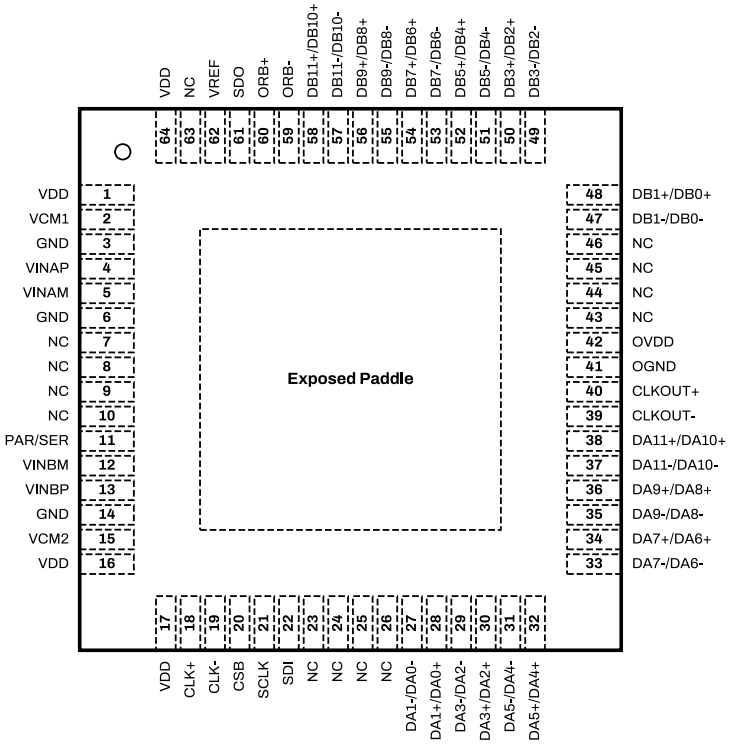



*Figure 7: SD2142ET Package Top View for Channel Multiplexed LVDS Configuration.*

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

*Table 13. Pin Descriptions for Channel Multiplexed LVDS Configuration.*

| Number | Name | Type | Comment |
|---|---|---|---|
| 0 | GND | Ground | Exposed Paddle, Analog Ground. |
| 1, 16, 17, 64 | VDD | Power | Analog Supply Voltage. |
| 2 | VCM1 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor. |
| 3, 6, 14 | GND | Ground | ADC Ground. |
| 4 | VINAP | Input | Differential Analog Input Pin (Plus) for Channel A. |
| 5 | VINAM | Input | Differential Analog Input Pin (Minus) for Channel A. |
| 7, 8, 9, 10, 23, 24, 25, 26, 43, 44, 45, 46, 63 | NC | | Do not connect. |
| 11 | PAR/SER | Input | Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCLK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCLK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal. |
| 12 | VINBM | Input | Differential Analog Input Pin (Minus) for Channel B. |
| 13 | VINBP | Input | Differential Analog Input Pin (Plus) for Channel B. |

| Number | Name | Type | Comment |
|---|---|---|---|
| 15 | VCM2 | Output | Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor. |
| 18 | CLK+ | Input | ADC Clock Input (Plus). |
| 19 | CLK- | Input | ADC Clock Input (Minus). |
| 20 | CSB | Input | SPI Chip Select (Active Low). |
| 21 | SCLK | Input | Serial interface clock input. |
| 22 | SDI | Input | In Serial Programming Mode, (PAR/SER = 0V), SDI Is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part. |
| 27 | DA1-/DA0- | Output | Channel A LVDS Output Data 0 and 1 (Minus). |
| 28 | DA1+/DA0+ | Output | Channel A LVDS Output Data 0 and 1 (Plus). |
| 29 | DA3-/DA2- | Output | Channel A LVDS Output Data 2 and 3 (Minus). |
| 30 | DA3+/DA2+ | Output | Channel A LVDS Output Data 2 and 3 (Plus). |
| 31 | DA5-/DA4- | Output | Channel A LVDS Output Data 4 and 5 (Minus). |
| 32 | DA5+/DA4+ | Output | Channel A LVDS Output Data 4 and 5 (Plus). |
| 33 | DA7-/DA6- | Output | Channel A LVDS Output Data 6 and 7 (Minus). |
| 34 | DA7+/DA6+ | Output | Channel A LVDS Output Data 6 and 7 (Plus). |
| 35 | DA9-/DA8- | Output | Channel A LVDS Output Data 8 and 9 (Minus). |
| 36 | DA9+/DA8+ | Output | Channel A LVDS Output Data 8 and 9 (Plus). |
| 37 | DA11-/DA10- | Output | Channel A LVDS Output Data 10 and 11 (Minus). |
| 38 | DA11+/DA10+ | Output | Channel A LVDS Output Data 10 and 11 (Plus). |
| 39 | CLKOUT- | Output | Inverted Version of CLKOUT+. |
| 40 | CLKOUT+ | Output | Data Output Clock. |
| 41 | OGND | Ground | Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin. |
| 42 | OVDD | Power | Digital I/O Supply. Bypass to ground with a 0.1µF ceramic capacitor. |
| 47 | DB1-/DB0- | Output | Channel B LVDS Output Data 0 and 1 (Minus). |
| 48 | DB1+/DB0+ | Output | Channel B LVDS Output Data 0 and 1 (Plus). |
| 49 | DB3-/DB2- | Output | Channel B LVDS Output Data 2 and 3 (Minus). |
| 50 | DB3+/DB2+ | Output | Channel B LVDS Output Data 2 and 3 (Plus). |
| 51 | DB5-/DB4- | Output | Channel B LVDS Output Data 4 and 5 (Minus). |
| 52 | DB5+/DB4+ | Output | Channel B LVDS Output Data 4 and 5 (Plus). |
| 53 | DB7-/DB6- | Output | Channel B LVDS Output Data 6 and 7 (Minus). |
| 54 | DB7+/DB6+ | Output | Channel B LVDS Output Data 6 and 7 (Plus). |
| 55 | DB9-/DB8- | Output | Channel B LVDS Output Data 8 and 9 (Minus). |
| 56 | DB9+/DB8+ | Output | Channel B LVDS Output Data 8 and 9 (Plus). |
| 57 | DB11-/DB10- | Output | Channel B LVDS Output Data 10 and 11 (Minus). |
| 58 | DB11+/DB10+ | Output | Channel B LVDS Output Data 10 and 11 (Plus). |
| 59 | ORB- | Output | Channel B LVDS Overflow Output (Minus). |
| 60 | ORB+ | Output | Channel B LVDS Overflow Output (Plus). |
| 61 | SDO | Output | In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part. |
| 62 | VREF | InOut | Voltage Reference Input/Output. |

## TYPICAL PERFORMANCE CHARACTERISTICS

*At $T_A$ = 25°C, $V_{VDD}$ = 1.8V, $V_{OVDD}$ = 1.8V, $F_{CLK}$ = 65MHz, $A_{IN}$ = -1dBFS, differential AC-coupled clock source, High-Performance Calibration Mode enabled, background calibration enabled, LVDS mode, unless otherwise noted.*

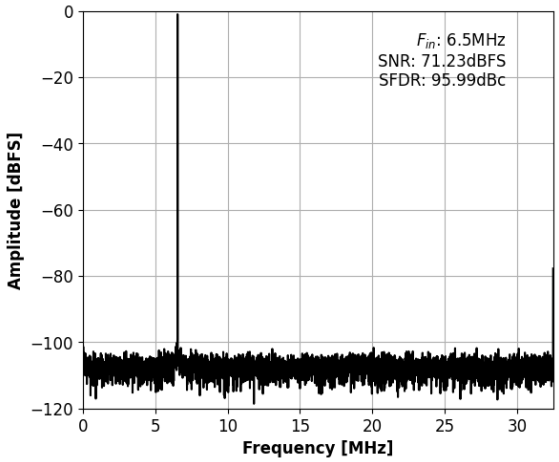



*Figure 8: Single-Tone FFT with $f_{IN}$=6.55MHz.*

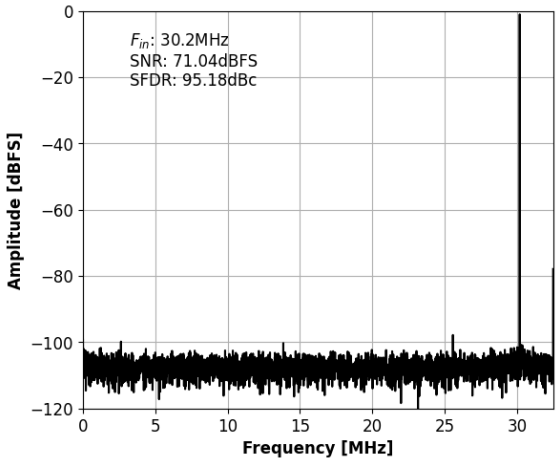



*Figure 9: Single-Tone FFT with $f_{IN}$=30.2MHz.*

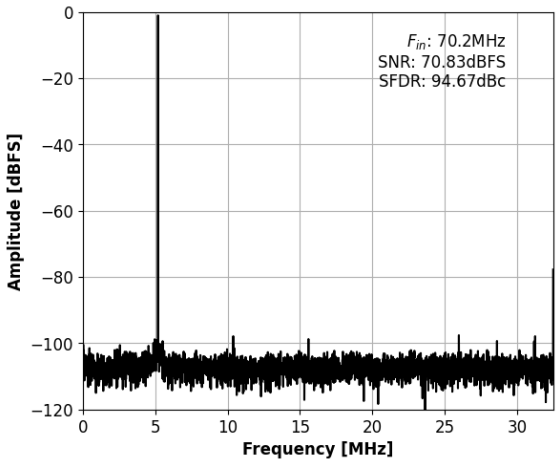



*Figure 10: Single-Tone FFT with $f_{IN}$=70.2MHz.*

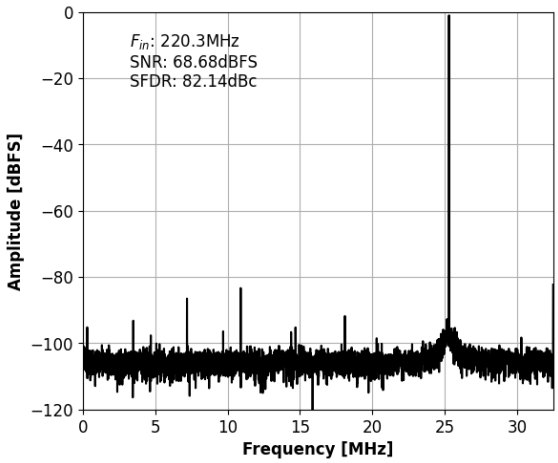



*Figure 11: Single-Tone FFT with $f_{IN}$=220MHz.*

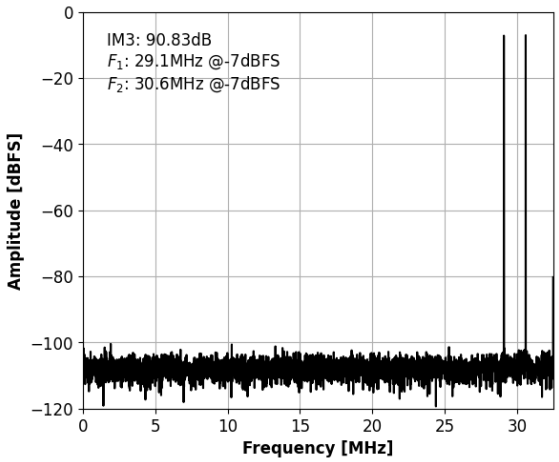



*Figure 12: Two-Tone FFT with $f_{IN1}$=29.1MHz, $f_{IN2}$=30.6MHz.*

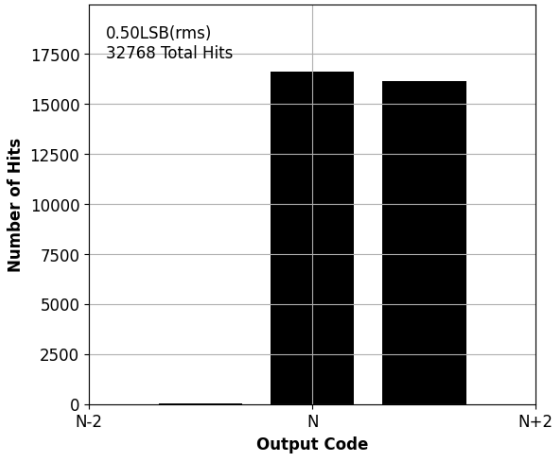



*Figure 13: Grounded Input Histogram.*

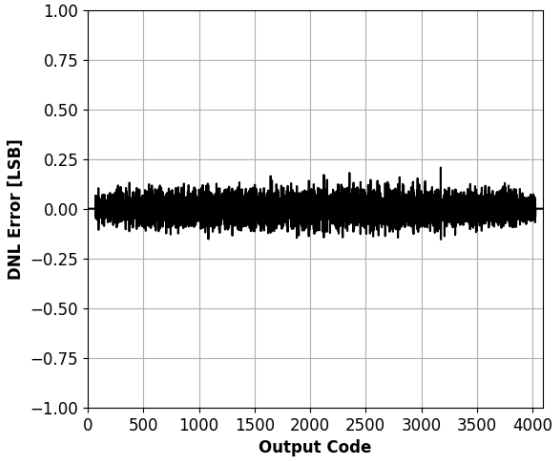



Figure 14: DNL Error with $f_{IN}$=6.55MHz.

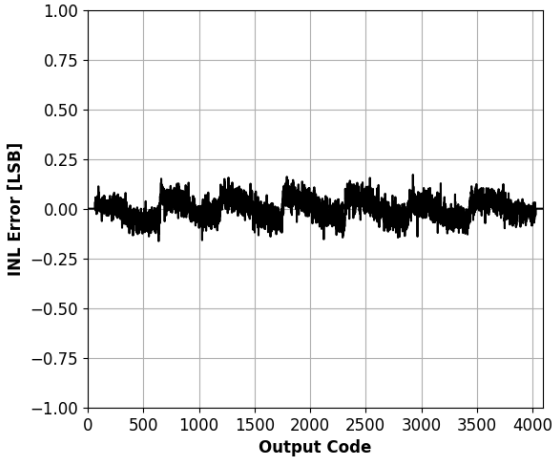



Figure 15: INL Error with $f_{IN}$=6.55MHz.

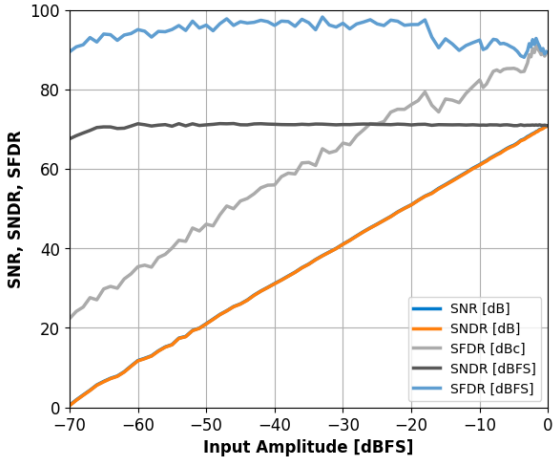



Figure 16: Single-Tone SNR, SNDR and SFDR vs. Input Amplitude with $f_{IN}$=30.25MHz.

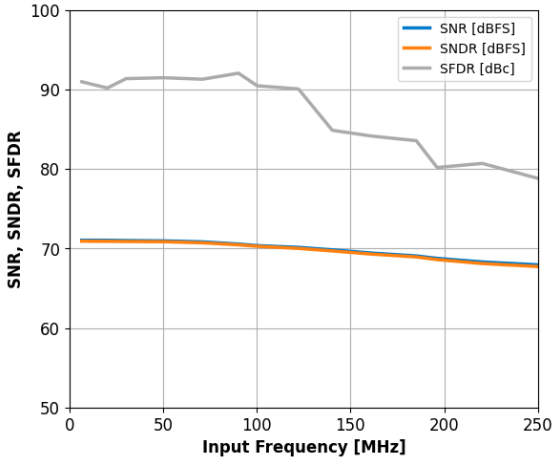



Figure 17: Single-Tone SNR, SNDR and SFDR vs. Input Frequency with $f_S$=65MHz.

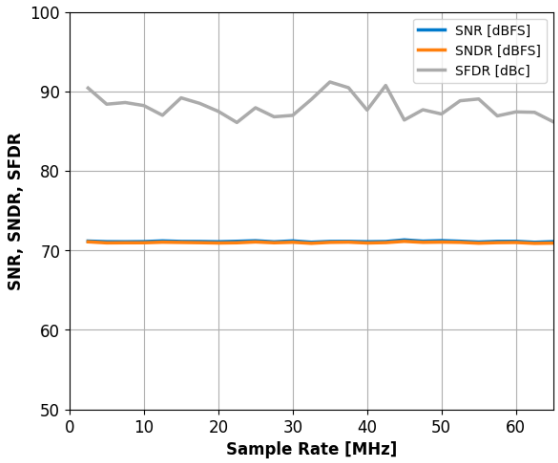



Figure 18: Single-Tone SNR, SNDR and SFDR vs. Sample Rate with $f_{IN}$=30.25MHz.

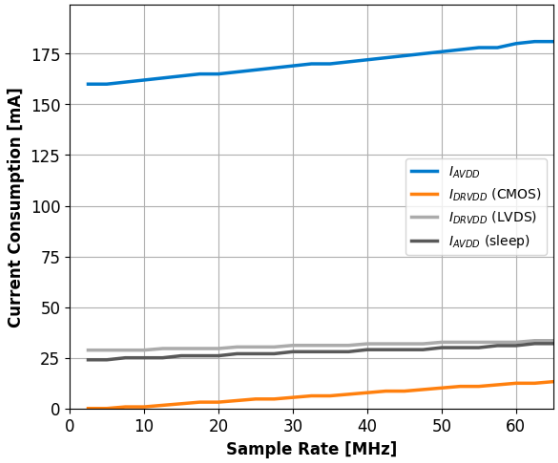



Figure 19: Current vs. Sample Rate.

## EQUIVALENT CIRCUITS

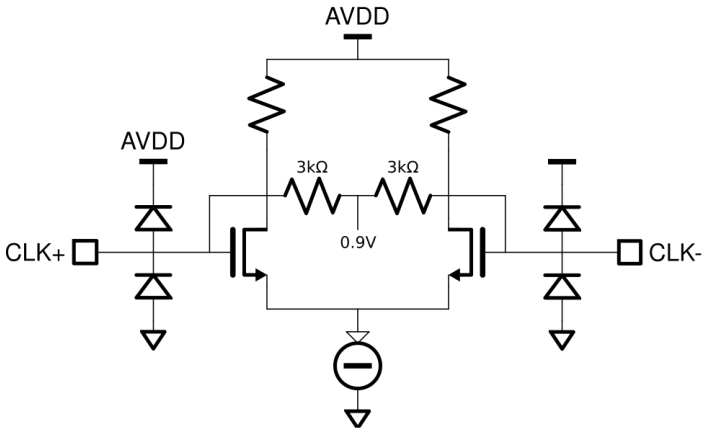



*Figure 20: Equivalent Clock Input Circuit.*

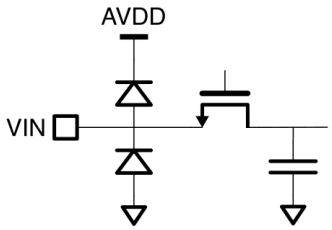



*Figure 21: Equivalent Analog Input Circuit.*

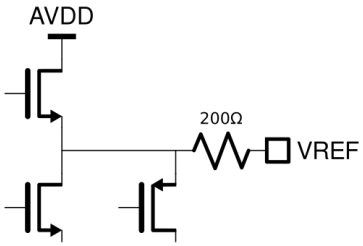



*Figure 22: Equivalent VREF Circuit.*

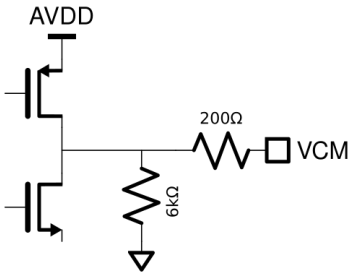



*Figure 23: Equivalent VCM Circuit.*

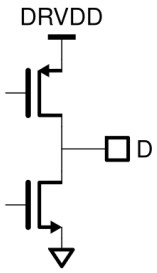



*Figure 24: Equivalent Digital Output Circuit.*

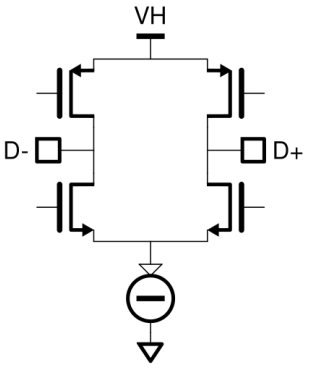



*Figure 25: Equivalent LVDS output Circuit.*

# THEORY OF OPERATION

## ADC Architecture

The ADC uses a pipelined architecture and innovative patented switched-capacitor circuits. Its fully differential design provides exceptional immunity to power supply noise and minimizes reference voltage self-modulation. A built-in Sample-and-Hold (S/H) function is integrated into the input stage of the pipeline structure.

## Analog Input

The input stage of the ADC behaves as a switched-capacitor network, presenting itself to the driving circuit as a combination of a switch and a sampling capacitor. The capacitor is reset prior to each conversion cycle, effectively eliminating non-linear memory effects commonly observed in some pipelined ADC architectures. The ADC does not include an internal common-mode bias therefore, the driving source must provide an appropiate common-mode voltage.

## Differential Clock Input

The SD2142ET features a differential clock receiver with an integrated common-mode bias. For proper operation, the clock inputs should be AC-coupled using 10nF capacitors.

**Differential Clock Configuration.** For optimal jitter performance, a differential clock source is recommended. The differential clock signals to CLK+ and CLK- should be connected through a 10nF AC-coupling capacitors.

**Single-Ended Clock Configuration.** If a single-ended clock source is used, the signal source should be AC-coupled to the CLK+ pin. In this configuration, a 10nF capacitor should be connected between the CLK- pin and analog ground to maintain proper biasing.

**Clock Jitter Considerations.** Clock jitter has a significant impact on the ADC's signal-to-noise ratio (SNR). The sensitivity to jitter increases with input signal frequency. For best performance, a low-noise differential clock with fast edge transitions should be used.

**Note**: The part can enter in manufacturing test mode if both differential clock inputs are held low for more than 1ms. This behavior can be prevented by writing 1 to register *0x4cf*, bit[15].

## Clock Divider

The ADC includes a programmable clock divider that allows the input clock to be divided by integer values from 2 to 8. The divider is configured by setting register *0x463*, bits [7:5], to the desired division value. A value of 0 (default) bypasses the divider entirely.

By default, the divider starts asynchronously.

**Clock Duty-Cycle Requirements.** The ADC utilizes both the rising and falling edges of the input clock (or the divided clock, if the divider is enabled) for internal sampling operations. To achieve optimal performance, especially at the maximum sampling rate, the clock duty cycle should be as close to 50% as possible.

When the divider is enabled with an even divisor, a 50% duty cycle is guaranteed by design. If the application uses a clock with a non-ideal duty cycle, a Duty Cycle Stabilizer (DCS) can be enabled to improve performance.

## ADC Self-Calibration

The ADC includes an automatic calibration mechanism that is executed at power-up to ensure optimal performance. It calibrates out capacitor mismatch and the effects of operational amplifier finite gain and bandwidth. For best results, calibration should be performed at the actual sampling rate used during operation. To support this, the device continuously monitors the sampling clock frequency and automatically re-triggers calibration if a significant change is detected. This feature can be disabled by setting register *0x4c9*, bit[0], to 1.

Manual calibration can also be initiated by toggling both *0xdc1*, bit[4] and *0xcc1*, bit[4] from 0 to 1. The calibration process is implemented using a state-machine architecture, ensuring a deterministic and predictable calibration time. By default the

calibration takes 46 million ADC sampling clock cycles. Calibration completion status can be read from *0xdef*, bit[0], for the first ADC and *0xcef*, bit[0], for the second ADC after the status readback is enabled by writing 0x1c to both *0xdeb* and *0xceb*. Bit value 1 indicates that calibration is complete.

In addition, the ADC supports a Background Calibration (BGC) mode, which is disabled by default. When enabled, parameters for compensating changes in operational amplifier gain and bandwidth are continuously updated. BGC is beneficial in environments with large temperature variations near the hot end of the specified operating temperature range. For its operation, BGC uses a dither signal which is injected into the ADC input signal path. This dither consumes approximately 0.8dB of the ADC's input range, resulting in earlier clipping compared to when BGC is disabled. When BGC is enabled calibration completion status bit remains 0.

To enable BGC:

- Write 0b01 to register 0xde1, bits [15:14]
- Write 0b01 to register 0xce1, bits [15:14]
- Write 0x0d80 to register 0xdcf
- Write 0x0d80 to register 0xccf
- Write 0b0 to register 0xde3, bit [3]
- Write 0b0 to register 0xce3, bit [3]

Calibration parameters can be altered to optimize ADC performance and the duration of the calibration according to Table 14.

High Performance settings improve the low frequency SFDR compared to the default settings while the High Speed Settings minimize the calibration time at the cost of small SFDR and SNDR degradation. If the parameters are altered, the calibration has to be reinitiated as described earlier.

*Table 14. Calibration Settings.*

| Register Address | Default Value | High Performance Value | High Speed Value |
|---|---|---|---|
| 0xccd | *0x1483* | *0x3483* | *0x348c* |
| 0xcd5 | *0x1483* | *0x3483* | *0x348c* |
| 0xcdd | *0x16c3* | *0x36c3* | *0x36cc* |
| 0xce1 | *0xbbe8* | *0xbb80* | *0xbb20* |
| 0xdcd | *0x1483* | *0x3483* | *0x348c* |
| 0xdd5 | *0x1483* | *0x3483* | *0x348c* |
| 0xddd | *0x16c3* | *0x36c3* | *0x36cc* |
| 0xde1 | *0xbbe8* | *0xbb80* | *0xbb20* |
| Duration (clock cycles) | 46M | 25M | 6.3M |

## Stand-by and Power-Down Modes

The SD2142ET supports two power-saving modes, power down and stand-by, that can be used when the ADCs are not actively sampling. In both modes, the SPI interface (if enabled) remains operational.

**Power-Down Mode.** This mode disables most of the internal circuitry, resulting in the lowest residual supply current. It is ideal for applications requiring minimal power consumption during idle periods. Power-down mode can be enabled via:

- The PDWN pin when operating in the external pin mode, or
- Setting register *0x457*, bit[7], to 1.

**Stand-by Mode.** Stand-by mode offers a faster wake-up time compared to power-down mode, at the cost of slightly higher residual current. It is suitable for applications that require rapid recovery from idle states. To enable stand-by mode, set register *0x457*, bits [3] and [8], to 1.

**Note**: It is recommended to disable the ADC auto-calibration when using stand-by mode to avoid unintended calibration

cycles during transitions.

## Commonly Used Functions

The SD2142ET offers several functions available via dual function pin controls (external pin mode vs. SPI mode). The SD2142ET detects the SPI mode during the first SPI transaction after power-up. If the user does not want to program the device via the SPI interface, the dual function is available.

**Duty-Cycle Stabilizer**. The Duty-Cycle Stabilizer (DCS) retimes the falling edge of the clock thus providing an internal clock signal with a 50% duty cycle. The DCS is useful in systems where the input clock has an uneven duty cycle. It can be enabled via register control, by setting register *0x457*, bit[1], to 1.

**Output Enable** (active-low, **OEB**). The output data drivers can be placed in a high-impedance state using the OEB function, accessed by setting register *0x457*, bit[3], to 1.

**Common-Mode Voltage.** The VCM pin outputs the analog input common-mode bias voltage (VCM). This pin provides a stable DC reference that can be used to set the ADC input common-mode level, either directly through a passive network or indirectly as the common-mode reference for a driving amplifier. In typical applications, the default common-mode voltage is suitable and requires no adjustment. The common-mode voltage level is programmable through register *0xf11*, bits [4:3].

**VREF.** The ADC supports both internal (default) and external voltage reference sources, selectable via the VREF pin.

The selection between internal and external reference voltage is via made register control: setting register *0x45d*, bit[5], to 1 selects the external reference.

Internal Reference Output. When the internal voltage reference is used, the VREF pin can function as a reference output. This output can be enabled by setting register *0x45d*, bits [14:13], to 0x3.

**Overrange Indicator.** This output bit indicates that the analog input sample exceeded the converter's full-scale input range. When the input signal exceeds the converter's positive (or negative) full-scale range, the ADC will clip, and the output data will saturate to the maximum (or minimum) digital code. In either case, the OR bit will be set, indicating that the input had been out of range during that sample.

The internal vref can be adjusted with *0x45d* bits [4:1]. Usually, the default value yields the optimal performance.

## SERIAL PORT INTERFACE

The SD2142ET uses a 4-wire Serial Port Interface (SPI) that gives the user flexibility to configure the converter for specific functions, depending on the application, through a register space provided inside the ADC. The interface signals are:

- SCLK: defines the bit rate at which serial data is driven onto, and sampled from, the bus;
- CSB: defines the boundaries of a basic data 'unit', comprised of multiple serial bits;
- SDI: is the serial data input wire;
- SDO: is the serial data output wire;

The read and write cycles are described in the figure below. The address space is 13 bits long (A<12:0>) and the data is 16 bits wide (D<15:0>). The complete instruction cycle is 32-bits long. The falling edge of CSB combines with the rising edge of SCLK marks the start of the instruction cycle. On a write transaction, the target register is updated on the falling edge of SCLK.

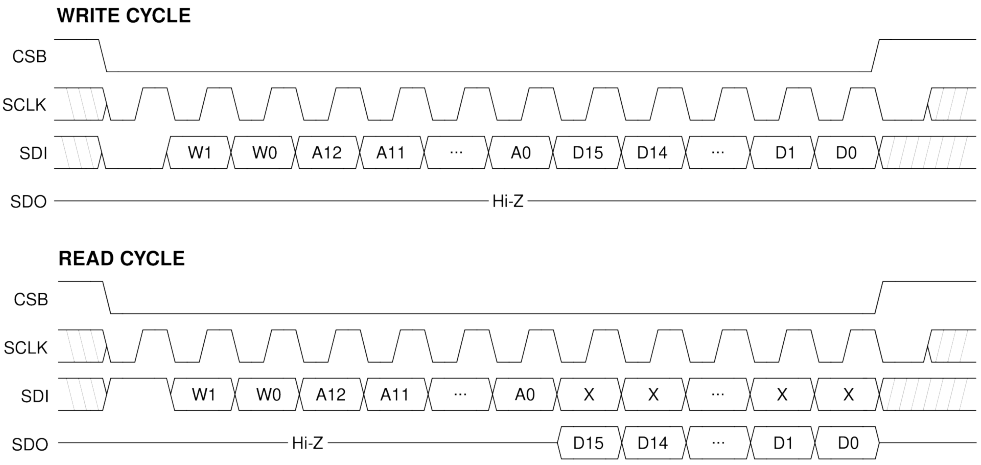



*Figure 26: 4-wire SPI timing.*

*Table 15. SPI Timing.*

| PARAMETER | TEMP | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Setup time between the data and the rising edge of SCLK | $t_{DS}$ | 2 | | | ns |
| Hold time between the data and the rising edge of SCLK | $t_{HD}$ | 2 | | | ns |
| Period of the SCLK | $t_{SCLK}$ | 40 | | | ns |
| Setup time between CSB and SCLK | $t_{S,CSB-SCLK}$ | 2 | | | ns |
| Hold time between CSB and SCLK | $t_{H,CSB-SCLK}$ | 2 | | | ns |
| Minimum period that SCLK should be in a logic high state | $t_{SCLK,high}$ | 10 | | | ns |
| Minimum period that SCLK should be in a logic high state | $t_{SCLK,low}$ | 10 | | | ns |

Two bits, W1 and W0, determine how many bytes of data that can be transferred in the same write cycle (see Table 16). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.

*Table 16. SPI Word Length.*

| [W1,W0] | Data length |
|---|---|
| 00 | Not supported |
| 01 | Two bytes of data can be transferred |
| 10 | Not supported |
| 11 | Four bytes of data can be transferred |

The SPI pins should not be active when the full dynamic performance of the ADC is required. Noise from SCLK, CSB and the data transactions can degrade ADC performance.

# OUTPUT MODE

## Data Scrambler

Interference originating from the digital outputs of the ADC can be difficult to eliminate entirely. Such interference may result from capacitive or inductive coupling mechanisms, or from shared impedance paths in the ground plane. Even minimal coupling coefficients can introduce deterministic spurious tones into the ADC's output frequency spectrum. To mitigate this, digital output scrambling techniques can be employed prior to off-chip transmission. By randomizing the bit patterns, the spectral energy of these spurs is dispersed, effectively reducing their peak amplitudes and minimizing their impact on signal integrity.

The SD2142ET can apply an exclusive-OR logic operation between the LSB and all other data output bits, while the LSB, overflow and clock outputs are not affected.

When this function is used, the receiver must apply the same function to unscramble the received data.

The data scrambler is enabled by setting control register *0x4b5*, bit[13], to 1.

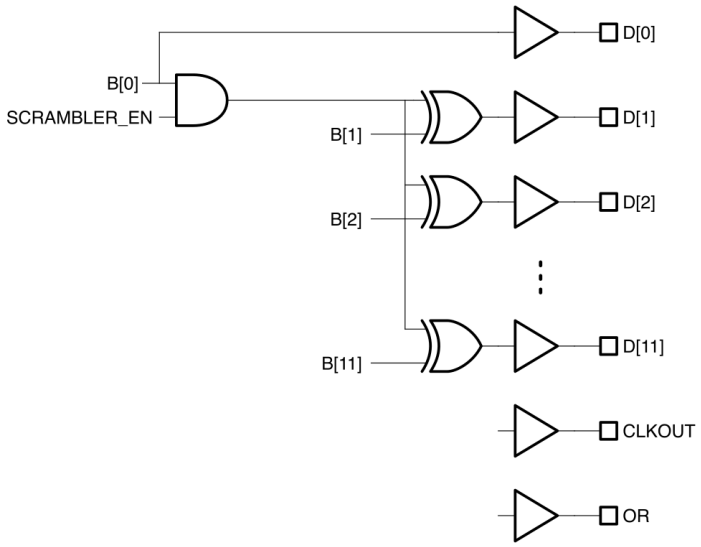



*Figure 27: SD2142ET Data Scrambler.*

## Alternate Bit Polarity

The alternate bit polarity is particularly effective to suppress digital feedback and minimize noise coupling on the PCB when the ADC input signal is near mid-scale and of very small amplitude. In this case, the digital output tends to toggle between patterns dominated by either logic high or logic low states. This synchronized switching of multiple bits can induce significant transient currents in the ground plane, leading to increased digital noise. This mode, when activated, inverts all odd-numbered data output bits prior to the output buffer stage while even-numbered bits, along with the overflow and clock output, remain unaffected thus ensuring that approximately half of the output bits transition are high while the other half transition are low. This balanced switching behavior helps cancel out opposing current flows in the ground return path, thereby reducing overall ground noise. At the receiving end, the original data can be reconstructed by inverting the same odd-numbered bits. This mode operates independently of the digital output randomization feature, both functions can be enabled or disabled separately. The Alternate Bit Polarity mode is configured via serial programming of control register *0x4b5*, bit[14].

## Output Test Modes

The output test options are described in Table 17 and are selected via SPI programming at register *0x4b5*, bits [5:2].

When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. These tests require an active input clock.

There are two pseudo-random number generators available, PN23 and PN9. The PN23 generator ($X^{23}+X^{18}+1$), selected by register *0x4b5*, bits [5:2], set to 0x5, can be reset by setting register *0x4b5*, bit [12], low; while the PN9 generator ($X^{9}+X^{5}+1$), selected by register *0x4b5* set to 0x6, can be reset by setting register *0x4b5*, bit [11], low.

*Table 17. Output Test Modes.*

| Mode | Function |
|---|---|
| 0 | Pass-Through |
| 1 | Midscale |
| 2 | +FS |
| 3 | -FS |
| 4 | Checkerboard |
| 5 | PN23 |
| 6 | PN9 |
| 7 | 1/0 word toggle |
| 8 | User input |
| 9 | 1/0 bit toggle |
| 10 | Unused |
| 11 | 1-bit high |
| 12 | Mixed frequency |
| 13 | Unused |
| 14 | Unused |
| 15 | Ramp |

Pass-through and test patterns 1, 2, 3, 5 and 6 are subject to output formatting, while the other test modes are not. Test patterns 1 to 8 and 15 can be applied to either one channel or both channels using *0x4b5*, bit[7:6]. Patterns 4 and 7 can be toggled between the pattern and its inverse while test pattern 8 can be selected using registers *0x4bb*, *0x4bd*, *0x4bf* and *0x4c1*.

## Inverting the Channel Polarity

The following writes must be executed in order and after the sampling clock is asserted:

*Table 18. Output Polarity Inversion (ADC_B only).*

| Register | Value |
|---|---|
| 0x0807 | 0x0101 |
| 0x0813 | 0x58AB |
| 0x082B | 0x0001 |
| 0x082B | 0x0000 |
| 0x0807 | 0x0100 |
| 0x0813 | 0x58EB |

## CONTROL REGISTERS

This section describes the most commonly used control registers. For a description of the complete register map, refer to Appendix A: Register Map.

Each register is presented in the following format:

| **Address: <HEX value>** | | **RW** or **RO** | **Default: <HEX value>** |
|---|---|---|---|
| bit field | default value | field description. | |

### Notes

- **RW** = Read/Write
- **RO** = Read-Only
- For read-only registers, the default value is omitted.
- Registers not listed in these tables should not be written.

When updating control register values, always use a read-modify-write procedure. Some registers include reserved bit fields for internal engineering purposes. This approach ensures that these reserved bits remain unchanged and prevents unintended modifications.

**CHIP TOP**:

| **Address: 0x457** | | **RW** | **Default: 0x0015** |
|---|---|---|---|
| [0] | 0x1 | Duty Cycle Stabilizer enable (see Duty-Cycle Stabilizer).<br>0: Disable<br>1: Enable | |
| [1] | 0x0 | Duty Cycle Stabilizer on/off in SPI mode (see Duty-Cycle Stabilizer).<br>0: Off<br>1: On | |
| [2] | 0x1 | External output enable (OE/OEB) control (see Output Enable).<br>0: Output Enabled<br>1: Output depends on pin OE/OEB | |
| [3] | 0x0 | Output disable (see Output Enable).<br>0: Output depends on OE/OEB control and OE/OEB pin<br>1: Disabled | |
| [6:4] | 0x1 | Reserved. | |
| [7] | 0x0 | Software power down.<br>0: Active State<br>1: Power Down | |
| [8] | 0x0 | Software stand-by mode.<br>0: Active State<br>1: Stand-by Mode | |

| Address: 0x463 | | RW | Default: 0x0019 |
|---|---|---|---|
| [0] | 0x1 | Enable clock receiver.<br>0: Disable<br>1: Enable | |
| [4:1] | 0xc | Reserved. | |
| [7:5] | 0x0 | Clock RX divider control.<br>0: Bypass<br>1: Divide by 2<br>2: Divide by 3<br>3: Divide by 4<br>4: Divide by 5<br>5: Divide by 6<br>6: Divide by 7<br>7: Divide by 8 | |
| [8] | 0x0 | Enable on-chip 100Ohm termination.<br>0: Disable<br>1: Enable | |
| [9] | 0x0 | Clock polarity control when DCS is enabled.<br>0: Disable<br>1: Invert | |
| [10] | 0x0 | Reserved. | |

| Address: 0x473 | | RW | Default: 0x0000 |
|---|---|---|---|
| [4:0] | 0x0 | Reserved. | |
| [8:5] | 0x0 | Output data delay in parallel CMOS mode.<br>The output data delay (250ps steps) with respect to the clock | |
| [9] | 0x0 | Launching output clock polarity in parallel CMOS mode.<br>0: Not inverted<br>1: Inverted | |
| [13:10] | 0x0 | Output clock delay.<br>The output clock delay is increased by 250ps * (register value) with respect to the data | |
| [14] | 0x0 | Output clock polarity.<br>0: Not inverted<br>1: Inverted | |

| Address: 0x4b5 | | RW | Default: 0x18c0 |
|---|---|---|---|
| [1:0] | 0x0 | Output format.<br>0: Offset binary<br>1: Two's complement<br>2: Gray code<br>3: Offset binary | |
| [5:2] | 0x0 | Output test mode select (see Table 17). | |
| [6] | 0x1 | Output test channel CH. A<br>0: Disable<br>1: Enable | |
| [7] | 0x1 | Output test channel CH. B<br>0: Disable<br>1: Enable | |
| [8] | 0x0 | Output test toggle mode. Toggle between user test pattern 0 and 1. | |
| [10:9] | 0x0 | Reserved. | |
| [11] | 0x1 | PN9 generator reset (active low). | |
| [12] | 0x1 | PN23 generator reset (active low). | |
| [13] | 0x0 | Enable the output data scrambler.<br>0: Disable<br>1: Enable | |
| [14] | 0x0 | Enable alternate bit polarity switch.<br>0: Disable<br>1: Enable | |

| Address: 0x503 | | RW | Default: 0x0000 |
|---|---|---|---|
| [1:0] | 0x0 | Serial Mode Interface Setup:<br>0: Full Rate CMOS Interface<br>1: DDR LVDS Interface<br>2: DDR CMOS Interface<br>3: Not Used | |

**ADC A**:

| Address: 0xdc1 | | RW | Default: 0xbfff |
|---|---|---|---|
| [3:0] | 0xf | Reserved. | |
| [4] | 0x1 | Calibration soft reset (active low). | |
| [15:5] | 0x5f9 | Reserved. | |

See Table 14 for valid configurations for the following registers:

| Address: 0xdcd | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stg1 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stg1 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xdd5 | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 2 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stage 2 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xddd | | RW | Default: 0x16c3 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 3 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0xd8 | Reserved. | |
| [13:12] | 0x1 | Stage 3 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xde1 | | RW | Default: 0xbae8 |
|---|---|---|---|
| [7:0] | 0xe8 | Time allocated for calibration (see Table 14). | |
| [8] | 0x0 | Enable calibration (see Table 14). | |
| [9] | 0x1 | Enable foreground calibration (see Table 14). | |
| [10] | 0x0 | Reserved. | |
| [11] | 0x1 | Enable stg1 calibration (see Table 14). | |
| [12] | 0x1 | Enable stage 2 calibration (see Table 14). | |
| [13] | 0x1 | Enable stage 3 calibration (see Table 14). | |
| [14] | 0x0 | Background calibration parallel mode (see Table 14). | |
| [15] | 0x1 | Disable background calibration mode for all stages (see Table 14). | |

**ADC B**:

| Address: 0xcc1 | | RW | Default: 0xbfff |
|---|---|---|---|
| [3:0] | 0xf | Reserved. | |
| [4] | 0x1 | Calibration soft reset (active low). | |
| [15:5] | 0x5f9 | Reserved. | |

See Table 14 for valid configurations for the following registers:

| Address: 0xccd | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stg1 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stg1 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xcd5 | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 2 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stage 2 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xcdd | | RW | Default: 0x16c3 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 3 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0xd8 | Reserved. | |
| [13:12] | 0x1 | Stage 3 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xce1 | | RW | Default: 0xbae8 |
|---|---|---|---|
| [7:0] | 0xe8 | Time allocated for calibration (see Table 14). | |
| [8] | 0x0 | Enable calibration (see Table 14). | |
| [9] | 0x1 | Enable foreground calibration (see Table 14). | |
| [10] | 0x0 | Reserved. | |
| [11] | 0x1 | Enable stg1 calibration (see Table 14). | |
| [12] | 0x1 | Enable stage 2 calibration (see Table 14). | |
| [13] | 0x1 | Enable stage 3 calibration (see Table 14). | |
| [14] | 0x0 | Background calibration parallel mode (see Table 14). | |
| [15] | 0x1 | Disable background calibration mode for all stages (see Table 14). | |

## ADC BRING-UP

The SD2142ET does not require a specific power-up sequence; however, it is recommended to apply the OVDD first followed by the VDD.

## Extended Temperature

To maintain full ADC performance over the extended temperature range, background calibration must be enabled. The registers in Table 19 must be programmed via the SPI interface:

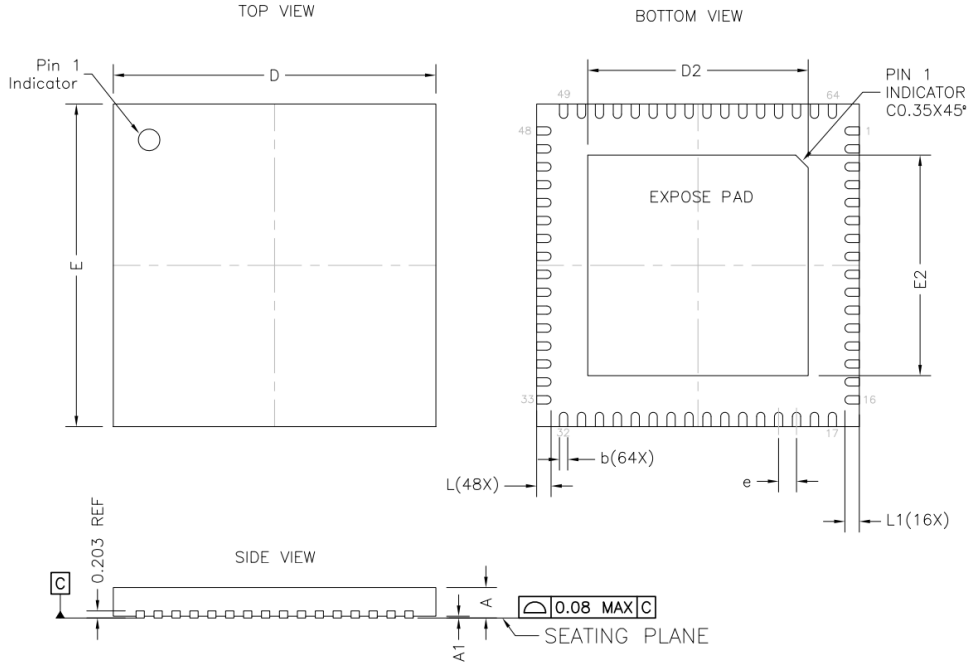
*Table 19. Background Calibration Enable.*

| Register Address | Value |
|---|---|
| *0xdcf* | 0xd80 |
| *0xccf* | 0xd80 |
| *0xde1* | 0xfb80 |
| *0xce1* | 0xfb80 |
| *0xde3* | 0x0 |
| *0xce3* | 0x0 |
| *0x809* | 0x18d4 |
| *0x80b* | 0x18d4 |

## ORDERING INFORMATION

This product is protected by several U.S. Patents (www.silannasemi.com/patents).

## PACKAGE DRAWING




| DIMENSION TABLE | | | |
|---|---|---|---|
| SYMBOL | MINIMUM | NOMINAL | MAXIMUM |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| D | 8.90 | 9.00 | 9.10 |
| D2 | 6.10 | 6.15 | 6.20 |
| E | 8.90 | 9.00 | 9.10 |
| E2 | 6.10 | 6.15 | 6.20 |
| e | | 0.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0.33 | 0.38 | 0.43 |

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5–2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pas as well as the terminals
5. Lead Finish: 100% Sn

*Figure 28: Package Dimensions.*

# APPENDIX A: Register Map

This section provides a comprehensive description of the complete register map, detailing all available control and status registers within the device.

## 0x400 - CHIP_TOP

| Address: 0x455 | | RW | Default: 0x0001 |
|---|---|---|---|
| [0] | 0x1 | Soft reset (active low). | |

| Address: 0x457 | | RW | Default: 0x0015 |
|---|---|---|---|
| [0] | 0x1 | Duty Cycle Stabilizer enable (see Duty-Cycle Stabilizer).<br>0: Disable<br>1: Enable | |
| [1] | 0x0 | Duty Cycle Stabilizer on/off in SPI mode (see Duty-Cycle Stabilizer).<br>0: Off<br>1: On | |
| [2] | 0x1 | External output enable (OE/OEB) control (see Output Enable).<br>0: Output Enabled<br>1: Output depends on pin OE/OEB | |
| [3] | 0x0 | Output disable (see Output Enable).<br>0: Output depends on OE/OEB control and OE/OEB pin<br>1: Disabled | |
| [6:4] | 0x1 | Reserved. | |
| [7] | 0x0 | Software power down.<br>0: Active State<br>1: Power Down | |
| [8] | 0x0 | Software stand-by mode.<br>0: Active State<br>1: Stand-by Mode | |

| Address: 0x45d | | RW | Default: 0x0095 |
|---|---|---|---|
| [0] | 0x1 | ADC reference voltage enable.<br>0: Disabled<br>1: Enabled | |
| [4:1] | 0xa | ADC reference voltage value.<br>0: Lowest<br>...<br>15: Highest | |
| [5] | 0x0 | Set reference.<br>0: Internal<br>1: External from VREF pin | |
| [11:6] | 0x2 | Reserved. | |
| [12] | 0x0 | Enable selection between Internal and External VREF selection via bit 5.<br>0: Bit [5] selection disabled<br>1: Bit [5] selection enabled | |
| [13] | 0x0 | Enable selection of VREF out via bit 14.<br>0: Bit [14] selection disabled<br>1: Bit [14] selection enabled | |
| [14] | 0x0 | Enable VREF pin as reference voltage output.<br>0: Disabled<br>1: Enabled | |

| Address: 0x463 | | RW | Default: 0x0019 |
|---|---|---|---|
| [0] | 0x1 | Enable clock receiver.<br>0: Disable<br>1: Enable | |
| [4:1] | 0xc | Reserved. | |
| [7:5] | 0x0 | Clock RX divider control.<br>0: Bypass<br>1: Divide by 2<br>2: Divide by 3<br>3: Divide by 4<br>4: Divide by 5<br>5: Divide by 6<br>6: Divide by 7<br>7: Divide by 8 | |
| [8] | 0x0 | Enable on-chip 100Ohm termination.<br>0: Disable<br>1: Enable | |
| [9] | 0x0 | Clock polarity control when DCS is enabled.<br>0: Disable<br>1: Invert | |
| [10] | 0x0 | Reserved. | |

| Address: 0x467 | | RW | Default: 0x3850 |
|---|---|---|---|
| [0] | 0x0 | Reserved. | |
| [1] | 0x0 | LVDS reduced swing mode.<br>0: Disable<br>1: Enable | |
| [5:2] | 0x4 | Reserved. | |
| [6] | 0x1 | LVDS bias enable.<br>0: Disable<br>1: Enable | |
| [10:7] | 0x0 | Reserved. | |
| [13:11] | 0x7 | LVDS amplitude.<br>0: Smallest amplitude<br>0: ...<br>7: Largest amplitude | |
| [15:14] | 0x0 | Reserved. | |

| Address: 0x473 | | RW | Default: 0x0000 |
|---|---|---|---|
| [4:0] | 0x0 | Reserved. | |
| [8:5] | 0x0 | Output data delay in parallel CMOS mode.<br>The output data delay (250ps steps) with respect to the clock | |
| [9] | 0x0 | Launching output clock polarity in parallel CMOS mode.<br>0: Not inverted<br>1: Inverted | |
| [13:10] | 0x0 | Output clock delay.<br>The output clock delay is increased by 250ps * (register value) with respect to the data | |
| [14] | 0x0 | Output clock polarity.<br>0: Not inverted<br>1: Inverted | |

| Address: 0x475 | | RW | Default: 0x0001 |
|---|---|---|---|
| [0] | 0x1 | Enable VCM.<br>0: Disable<br>1: Enable | |

| Address: 0x4b5 | | RW | Default: 0x18c0 |
|---|---|---|---|
| [1:0] | 0x0 | Output format.<br>0: Offset binary<br>1: Two's complement<br>2: Gray code<br>3: Offset binary | |
| [5:2] | 0x0 | Output test mode select (see Table 17). | |
| [6] | 0x1 | Output test channel CH. A<br>0: Disable<br>1: Enable | |
| [7] | 0x1 | Output test channel CH. B<br>0: Disable<br>1: Enable | |
| [8] | 0x0 | Output test toggle mode. Toggle between user test pattern 0 and 1. | |
| [10:9] | 0x0 | Reserved. | |
| [11] | 0x1 | PN9 generator reset (active low). | |
| [12] | 0x1 | PN23 generator reset (active low). | |
| [13] | 0x0 | Enable the output data scrambler.<br>0: Disable<br>1: Enable | |
| [14] | 0x0 | Enable alternate bit polarity switch.<br>0: Disable<br>1: Enable | |

| Address: 0x4b7 | | RW | Default: 0x0092 |
|---|---|---|---|
| [15:0] | 0x0092 | PN9 initial seed. | |

| Address: 0x4b9 | | RW | Default: 0x3aff |
|---|---|---|---|
| [15:0] | 0x3aff | PN23 initial seed. | |

| Address: 0x4bb | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | User test pattern 0 (CH. A). | |

| Address: 0x4bd | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | User test pattern 1 (CH. A). | |

| Address: 0x4bf | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | User test pattern 0 (CH. B). | |

| Address: 0x4c1 | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | User test pattern 1 (CH. B). | |

| Address: 0x4c9 | | RW | Default: 0x0000 |
|---|---|---|---|
| [0] | 0x0 | Disable auto-recalibration.<br>0: Disable<br>1: Enable | |
| [15:1] | 0x0 | Reserved. | |

| Address: 0x4cf | | RW | Default: 0x0035 |
|---|---|---|---|
| [14:0] | 0x35 | Reserved. | |
| [15] | 0x0 | Disable production test mode.<br>0: Test mode enabled<br>1: Test mode disabled | |

| Address: 0x4d3 | | RW | Default: 0x0007 |
|---|---|---|---|
| [3:0] | 0x7 | LVDS common mode voltage. | |
| [7:4] | 0x0 | Reserved. | |

| Address: 0x4fd | RO | Default: N/A |
|---|---|---|
| [2:0] | Chip revision. | |
| [6:3] | Label ID. | |
| [8:7] | Reserved. | |
| [10:9] | Resolution ID for device<br>0: 10-bit<br>1: 12-bit<br>2: 14-bit<br>3: 16-bit | |
| [13:11] | Speed ID for device. | |

| Address: 0x4ff | RO | Default: N/A |
|---|---|---|
| [0] | Reserved. | |
| [1] | Analog Supply Ready.<br>0: Not ready<br>1: Ready | |
| [2] | Digital Supply Ready. | |
| [3] | I/O Supply Ready.<br>0: Not ready<br>1: Ready | |
| [4] | Reserved. | |
| [5] | SPI enabled.<br>0: Not enabled<br>1: Enabled | |
| [10:6] | Reserved. | |

| Address: 0x503 | | RW | Default: 0x0000 |
|---|---|---|---|
| [1:0] | 0x0 | Serial Mode Interface Setup:<br>0: Full Rate CMOS Interface<br>1: DDR LVDS Interface<br>2: DDR CMOS Interface<br>3: Not Used | |

## 0xF00 - ADC_DUAL

| Address: 0x809 | | RW | Default: 0x1800 |
|---|---|---|---|
| [11:0] | 0x800 | ADC A channel gain.<br>0x000: 0.0<br>0x800: 1.0<br>0xfff: 2.0 | |
| [12] | 0x1 | Enable ADC A path gain and offset. | |

| Address: 0x80b | | RW | Default: 0x1800 |
|---|---|---|---|
| [11:0] | 0x800 | ADC B channel gain.<br>0x000: 0.0<br>0x800: 1.0<br>0xfff: 2.0 | |
| [12] | 0x1 | Enable ADC B path gain and offset. | |

| Address: 0x80d | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | ADC A channel offset. Signed 16-bit two's complement number. | |

| Address: 0x80f | | RW | Default: 0x0000 |
|---|---|---|---|
| [15:0] | 0x0000 | ADC B channel offset. Signed 16-bit two's complement number. | |

| Address: 0xf03 | | RW | Default: 0x07f9 |
|---|---|---|---|
| [0] | 0x1 | Enable top level bias.<br>0: Disable<br>1: Enable | |
| [2:1] | 0x0 | Reserved. | |
| [3] | 0x1 | ADC_B enable.<br>0: Disable<br>1: Enable | |
| [4] | 0x1 | ADC_A enable.<br>0: Disable<br>1: Enable | |
| [10:5] | 0x3f | Mask for enable pin. | |

| Address: 0xf05 | | RW | Default: 0x0030 |
|---|---|---|---|
| [5:0] | 0x30 | Mask for stand-by pin. | |
| [6] | 0x0 | Stand-by ADC_B.<br>0: Disable<br>1: Enable | |
| [7] | 0x0 | Stand-by ADC_A.<br>0: Disable<br>1: Enable | |

| Address: 0xf07 | | RW | Default: 0x0043 |
|---|---|---|---|
| [0] | 0x1 | Digital clock enable.<br>0: Disable<br>1: Enable | |
| [1] | 0x1 | Analog clock enable.<br>0: Disable<br>1: Enable | |
| [2] | 0x0 | Reserved. | |
| [3] | 0x0 | Clock source select.<br>0: ADC_B<br>1: ADC_A | |
| [5:4] | 0x0 | Reserved. | |
| [6] | 0x1 | ADC clock generator reset (active low). | |
| [7] | 0x0 | Reserved. | |

| Address: 0xf11 | | RW | Default: 0x000b |
|---|---|---|---|
| [2:0] | 0x3 | Reserved. | |
| [4:3] | 0x1 | VCM voltage control.<br>0: Lowest common-mode voltage<br>...<br>3: Highest common-mode voltage | |

## 0xDC0 - ADC A

| Address: 0xdc1 | | RW | Default: 0xbfff |
|---|---|---|---|
| [3:0] | 0xf | Reserved. | |
| [4] | 0x1 | Calibration soft reset (active low). | |
| [15:5] | 0x5f9 | Reserved. | |

| Address: 0xdc9 | | RW | Default: 0x06a5 |
|---|---|---|---|
| [8:0] | 0xa5 | Reserved. | |
| [9] | 0x1 | Stg1 enable background mode. | |
| [11:10] | 0x1 | Reserved. | |

| Address: 0xdcd | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stg1 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stg1 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xdcf | | RW | Default: 0x0d85 |
|---|---|---|---|
| [2:0] | 0x5 | Stg1 calibration convergence speed in background mode (see Table 14). | |
| [11:3] | 0x1b0 | Reserved. | |

| Address: 0xdd1 | | RW | Default: 0x02a5 |
|---|---|---|---|
| [0] | 0x1 | Stage 2 gain error calibration enable. | |
| [1] | 0x0 | Stage 2 gain error calibration only. | |
| [8:2] | 0x29 | Reserved. | |
| [9] | 0x1 | Stage 2 enable background mode. | |
| [11:10] | 0x0 | Reserved. | |

| Address: 0xdd3 | | RW | Default: 0x0bc0 |
|---|---|---|---|
| [0] | 0x0 | Stage 2 force calibration data. | |
| [3:1] | 0x0 | Stage 2 calibration data register. | |
| [6:4] | 0x4 | Stage 2 bg calibration data register. | |
| [9:7] | 0x7 | Stage 2 fg calibration data register. | |
| [11:10] | 0x2 | Stage 2 calibration mode. | |
| [14:12] | 0x0 | Stage 2 capacitor select register. | |
| [15] | 0x0 | Stage 2 cal data magnitude. | |

| Address: 0xdd5 | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 2 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stage 2 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xdd7 | | RW | Default: 0x0001 |
|---|---|---|---|
| [2:0] | 0x1 | Stage 2 calibration convergence speed in background mode (see Table 14). | |
| [11:3] | 0x0 | Reserved. | |

| Address: 0xddd | | RW | Default: 0x16c3 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 3 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0xd8 | Reserved. | |
| [13:12] | 0x1 | Stage 3 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xde1 | | RW | Default: 0xbae8 |
|---|---|---|---|
| [7:0] | 0xe8 | Time allocated for calibration (see Table 14). | |
| [8] | 0x0 | Enable calibration (see Table 14). | |
| [9] | 0x1 | Enable foreground calibration (see Table 14). | |
| [10] | 0x0 | Reserved. | |
| [11] | 0x1 | Enable stg1 calibration (see Table 14). | |
| [12] | 0x1 | Enable stage 2 calibration (see Table 14). | |
| [13] | 0x1 | Enable stage 3 calibration (see Table 14). | |
| [14] | 0x0 | Background calibration parallel mode (see Table 14). | |
| [15] | 0x1 | Disable background calibration mode for all stages (see Table 14). | |

| Address: 0xde3 | | RW | Default: 0x0008 |
|---|---|---|---|
| [2:0] | 0x0 | Reserved. | |
| [3] | 0x1 | Clipping control to reserve some headroom for background calibration signals (active low). | |

| Address: 0xdeb | | RW | Default: 0x0000 |
|---|---|---|---|
| [0] | 0x0 | Calibration status.<br>0: Not done<br>1: Done | |
| [7:1] | 0x0 | Reserved. | |

| Address: 0xdef | | RO | Default: N/A |
|---|---|---|---|
| [0] | | Calibration complete. | |
| [15:1] | | Reserved. | |

## 0xCC1 - ADC B

| Address: 0xcc1 | | RW | Default: 0xbfff |
|---|---|---|---|
| [3:0] | 0xf | Reserved. | |
| [4] | 0x1 | Calibration soft reset (active low). | |
| [15:5] | 0x5f9 | Reserved. | |

| Address: 0xcc9 | | RW | Default: 0x06a5 |
|---|---|---|---|
| [8:0] | 0xa5 | Reserved. | |
| [9] | 0x1 | Stg1 enable background mode. | |
| [11:10] | 0x1 | Reserved. | |

| Address: 0xccd | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stg1 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stg1 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xccf | | RW | Default: 0x0d85 |
|---|---|---|---|
| [2:0] | 0x5 | Stg1 calibration convergence speed in background mode (see Table 14). | |
| [11:3] | 0x1b0 | Reserved. | |

| Address: 0xcd1 | | RW | Default: 0x02a5 |
|---|---|---|---|
| [0] | 0x1 | Stage 2 gain error calibration enable. | |
| [1] | 0x0 | Stage 2 gain error calibration only. | |
| [8:2] | 0x29 | Reserved. | |
| [9] | 0x1 | Stage 2 enable background mode. | |
| [11:10] | 0x0 | Reserved. | |

| Address: 0xcd5 | | RW | Default: 0x1483 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 2 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0x90 | Reserved. | |
| [13:12] | 0x1 | Stage 2 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xcd7 | | RW | Default: 0x0001 |
|---|---|---|---|
| [2:0] | 0x1 | Stage 2 calibration convergence speed in background mode (see Table 14). | |
| [11:3] | 0x0 | Reserved. | |

| Address: 0xcdd | | RW | Default: 0x16c3 |
|---|---|---|---|
| [2:0] | 0x3 | Stage 3 calibration convergence speed in foreground mode (see Table 14). | |
| [11:3] | 0xd8 | Reserved. | |
| [13:12] | 0x1 | Stage 3 calibration randomization sequence in foreground mode (see Table 14). | |

| Address: 0xce1 | | RW | Default: 0xbae8 |
|---|---|---|---|
| [7:0] | 0xe8 | Time allocated for calibration (see Table 14). | |
| [8] | 0x0 | Enable calibration (see Table 14). | |
| [9] | 0x1 | Enable foreground calibration (see Table 14). | |
| [10] | 0x0 | Reserved. | |
| [11] | 0x1 | Enable stg1 calibration (see Table 14). | |
| [12] | 0x1 | Enable stage 2 calibration (see Table 14). | |
| [13] | 0x1 | Enable stage 3 calibration (see Table 14). | |
| [14] | 0x0 | Background calibration parallel mode (see Table 14). | |
| [15] | 0x1 | Disable background calibration mode for all stages (see Table 14). | |

| Address: 0xce3 | | RW | Default: 0x0008 |
|---|---|---|---|
| [2:0] | 0x0 | Reserved. | |
| [3] | 0x1 | Clipping control to reserve some headroom for background calibration signals (active low). | |

| Address: 0xceb | | RW | Default: 0x0000 |
|---|---|---|---|
| [0] | 0x0 | Calibration status.<br>0: Not done<br>1: Done | |
| [7:1] | 0x0 | Reserved. | |

| Address: 0xcef | RO | Default: N/A |
|---|---|---|
| [0] | Calibration complete. | |
| [15:1] | Reserved. | |

## REVISION HISTORY

| Version | Date | Comment |
|---|---|---|
| 1.0 | April 9, 2026 | Initial Release. |
| 2.0 | July 8, 2026 | General QA improvements. |
| 3.0 | September 3, 2026 | Updated performance tables. |
| 4.0 | September 24, 2026 | Clarified register 0x473 description. Swapped channel A/B in package drawing. |
| | | |

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