SD7112 OVERVIEW

The SD7112 is the industry smallest, a single-channel, 12-bit, analog-to-digital converter (ADC) supporting sampling rates up to 80MSps. The device uses a multistage pipeline architecture to achieve high signal-to-noise ratio (SNR) and linearity, over wide input signal bandwidth. The SD7112 can be set to operate using either CMOS or LVDS output interface. Programming for configuration and control is accomplished using a 3-wire SPI-compatible serial bus. The digital output data can be programmed to be delivered in offset binary, twos complement format, or gray code.

The device includes a DSP block that features decimation, digital down conversion (DDC), and IQ mismatch correction.

FEATURES

- 8×8, 3.4mm×3.4mm BGA, with 0.4mm ball-pitch
- SNR: 71.5dBFS at f_{IN} = 30.2MHz and f_S = 80MSps
- SFDR: 89.0dBc at f_{IN} = 30.2MHz and f_S = 80MSps
- -148.4dBFS/Hz input-noise at f_{IN} = 30.2MHz and f_S = 80MSps
- 2.0V nominal input
- Typical power consumption: 200mW at 80MSps
- Integer 1-to-8 input clock divider (640MHz maximum input rate)
- Sample rates of up to 80MSps
- 1.8V analog supply voltage
- LVDS (ANSI-644 levels) outputs
- Internal ADC voltage reference
- ADC clock duty cycle correction
- Serial port control
- Decimation by 2, 4
- Digital Down-Conversion
- IQ Mismatch Correction
- Energy saving power-down modes

APPLICATIONS

- Communications
- General-purpose software radios
- Data acquisition systems (DAQ)
- Process control Systems
- Smart antenna systems
- Multimode digital receivers
- Ultrasound equipment
- Radar/LiDAR applications

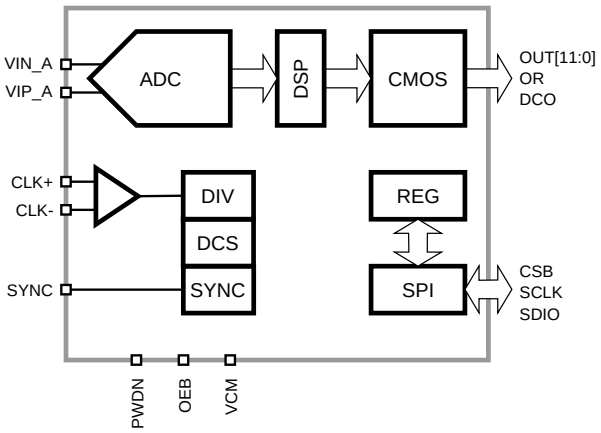


Figure 1: SD7112 Functional Block Diagram.

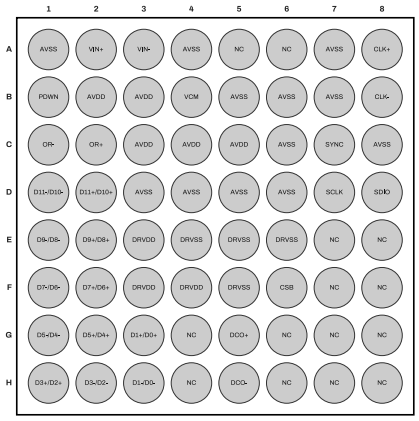


Figure 2: SD7112 8×8, BGA Package.

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SPECIFICATIONS

DC Specifications

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 80MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, LVDS mode, unless otherwise noted.

Table 1. DC Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Resolution			12		bits
Accuracy					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	-0.50		0.50	%FSR
Gain Error	Full	-3.00		2.00	%FSR
DNL	Full			±0.5	LSB
INL	Full			±0.8	LSB
Offset Error	25°C	-0.80		0.80	%FSR
Gain Error	25°C	-0.40		0.40	%FSR
Temperature Drift					
Offset Error	Full		+/-0.5		ppm/°C
Gain Error	Full		80.0		ppm/°C
Internal Voltage Reference					
Output Voltage	Full	1.02		1.07	V
External Voltage Reference					
Range	Full	0.90		1.07	V
Input Referred Noise					
V_{REF} = 1.0V	25°C		0.35		LSB(rms)
Analog Input					
Input Span, V_{REF} = 1.0V	Full		2.0		V
Input Capacitance	Full		6.0		pF
Input Resistance	Full		2.0		kΩ
Input Common-Mode Voltage	Full		0.70		V
Input Common-Mode Range	Full	0.62		0.93	V
VCM Voltage	Full		0.66		V
VCM Current Capability	Full		100		µA
Reference Input Resistance	Full		50		kΩ
Power Supply					
V_{AVDD}	Full	1.7	1.8	1.9	V
V_{DRVDD}	Full	1.7	1.8	1.9	V
I_{AVDD} @1.8V	Full		103	130	mA
I_{DRVDD} @1.8V (CMOS)	Full		8	11	mA
I_{DRVDD} @1.8V (LVDS)	Full		46	63	mA
Power Consumption					
Sine Wave Input (CMOS)	Full		200		mW
Sine Wave Input (LVDS)	Full		395		mW
Stand-by[1]	Full		60		mW
Power Down	Full		10.0		mW

[1] Stand-by power is measured with a sinewave input and active clock.

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AC Specifications

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 80MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

Table 2. AC Performance Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
f_{IN} = 6.55MHz	25°C		71.6		dBFS
f_{IN} = 30.2MHz	25°C		71.5		dBFS
	Full	70.3			dBFS
f_{IN} = 70.2MHz	25°C		71.2		dBFS
f_{IN} = 220MHz	25°C		68.9		dBFS
Signal-to-Noise and Distortion Ratio (SNDR)					
f_{IN} = 6.55MHz	25°C		71.2		dBFS
f_{IN} = 30.2MHz	25°C		71.2		dBFS
	Full	70.2			dBFS
f_{IN} = 70.2MHz	25°C		70.8		dBFS
f_{IN} = 220MHz	25°C		68.4		dBFS
Effective Number of Bits (ENOB)					
f_{IN} = 6.55MHz	25°C		11.5		bits
f_{IN} = 30.2MHz	25°C		11.5		bits
f_{IN} = 70.2MHz	25°C		11.5		bits
f_{IN} = 220MHz	25°C		11.1		bits
Worst 2nd or 3rd Harmonic Power					
f_{IN} = 6.55MHz	25°C		-89.3		dBc
f_{IN} = 30.2MHz	25°C		-89.2	-85.0	dBc
f_{IN} = 70.2MHz	25°C		-86.6		dBc
f_{IN} = 220MHz	25°C		-82.1		dBc
Worst Non-Harmonic Power					
f_{IN} = 6.55MHz	25°C		-93.0		dBc
f_{IN} = 30.2MHz	25°C		-91.0	-85.0	dBc
f_{IN} = 70.2MHz	25°C		-87.4		dBc
f_{IN} = 220MHz	25°C		-77.3		dBc
Spurious-Free Dynamic Range[1] (SFDR)					
f_{IN} = 6.55MHz	25°C		89.3		dBc
f_{IN} = 30.2MHz	25°C		89.0		dBc
	Full	82.0			dBc
f_{IN} = 70.2MHz	25°C		85.4		dBc
f_{IN} = 220MHz	25°C		75.3		dBc
Two-Tone SFDR					
f_{IN1} = 29.1MHz, f_{IN2} = 30.6MHz	25°C		90.4		dBc
Analog Input Bandwidth	Full		650.0		MHz

[1] SNR, SNDR and SFDR exclude the DC and f_S/2 bins.

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Digital Specification

V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 80MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, DCS disabled, unless otherwise noted.

Table 3. Differential Clock Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full		CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		1.2	V_{p-p}
Input Voltage Range	Full	V_{AVSS}-0.3		V_{AVDD}+0.2	V
Input Common-Mode Range	Full	0.75		1.05	V
High Level Input Current	Full	-10		10	µA
Low Level Input Current	Full	-10		10	µA
Input Capacitance	Full		1.7		pF
Input Resistance	Full		6.0		kΩ

Table 4. SYNC Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full		CMOS		
Input Voltage Range	Full	V_{AVSS}		V_{AVDD}	V
High Level Input Voltage	Full	1.22		V_{AVDD}	V
Low Level Input Voltage	Full	V_{AGND}		0.50	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 5. CSB Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 6. SCLK Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

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Table 7. SDIO Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 8. PDWN Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
Pull-down Current @1.8V	Full			90	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		28		kΩ

Table 9. CMOS Outputs (DATA and OR).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Output Voltage @50µA	Full	1.77			V
High Level Output Voltage @0.5mA	Full	1.75			V
Low Level Output Voltage @50µA	Full			0.05	V
Low Level Output Voltage @1.6mA	Full			0.10	V

Table 10. LVDS Outputs (DATA and OR).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	300	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.10	1.13	1.30	V
Differential Output Voltage (V_{OD}), Reduced Swing	Full	150	220	285	mV
Output Offset Voltage (V_{OS}), Reduced Swing	Full	1.10	1.22	1.30	V

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Switching Specifications

V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 80MHz, A_{IN} = -1dBFS, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.

Table 11. Clock Input Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Input Clock Rate	Full			640	MHz
Conversion Rate (after clock divider)	Full	10.0		80.0	MHz
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.5			ns
Divide-by-1 Mode, DCS Disabled	Full	5.6	6.2	6.8	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			ns
Aperture Delay (t_A)	Full		0.5		ns
Aperture Uncertainty (Jitter, t_J)	Full		140.0		fs

Table 12. SYNC Timing Requirements.

PARAMETER	MIN	TYP	MAX	UNIT
Set-Up Time ($t_{S,SYNC}$)		0.35		ns
Hold Time ($t_{H,SYNC}$)		0.35		ns

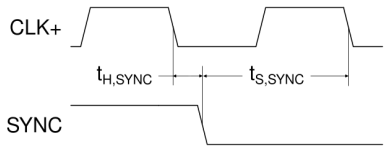


Figure 2: SYNC Input Timing.

Table 13. Data Output.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
CMOS Mode					
Data Propagation Delay (t_{PD})	Full		6.0		ns
DCO Propagation Delay (t_{DCO})	Full		7.0		ns
DCO to Data Skew (t_{SKEW})	Full	-1.1	-0.4	0.2	ns
Pipeline Delay (Latency, L)	Full		35.0		Cycles
LVDS Mode					
Data Propagation Delay (t_{PD})	Full		8.0		ns
DCO Propagation Delay (t_{DCO})	Full		7.7		ns
DCO to Data Skew (t_{SKEW})	Full	-1.1	-0.4	0.2	ns
Pipeline Delay (Latency, L) Channel A/Channel B	Full		32/32.5		Cycles
Wake-Up Time (from sleep)	Full		5.0		µs
Wake-Up Time (from power down)	Full		400.0		µs
Out-of-Range Recovery Time	Full		3		Cycles

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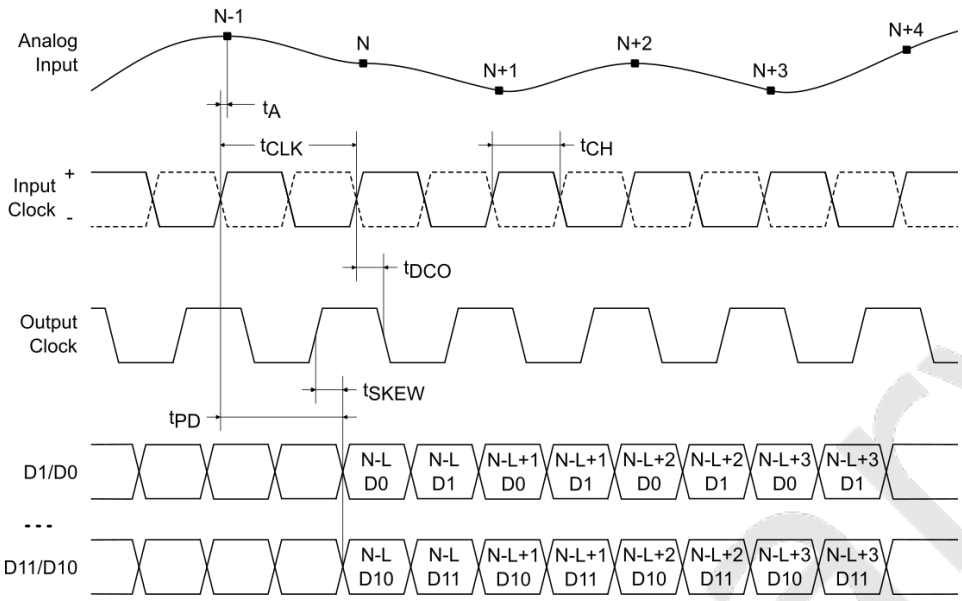


Figure 3: Channel Multiplexed LVDS Output Mode Timing.

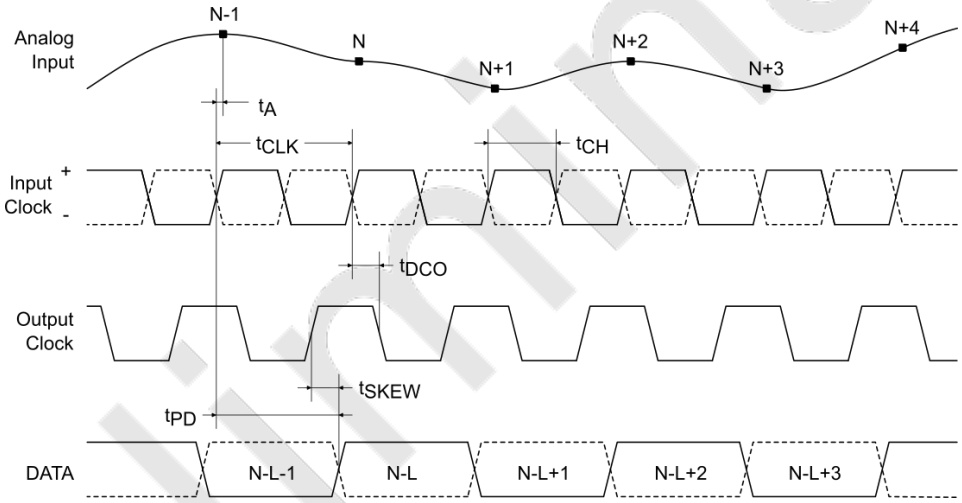


Figure 4: Parallel CMOS Output Mode Timing.

Output Modes

The SD7112 supports both CMOS and LVDS interfaces. Two LVDS samples are sent out every clock cycle using both the rising and the falling edge of the output clock. The even numbered bits are sent out on the first half-cycle and the odd bits on the second half-cycle. Register *0x465*, bits [2:0], controls the multiplexing (even/odd vs. odd/even, see register description for details).

Output Timing Control

Data delay control, bits [8:5], in register *0x473*, can be used to move the CMOS data relative to output clock. Bit [9] inverts the internal clock sending the data out. Bits [13:10], in register *0x473*, control the output clock delay relative to output data, while bit [14] inverts the clock. The delay step size is about 250ps.

Data delay control is not available in interleaved or multiplexed output mode.

Driving long traces or large load capacitance with CMOS output produces voltage ripple in the digital IO supply and ground, which may couple on chip to the sensitive analog circuits in the ADC and degrade the performance. This effect can be

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reduced by using an external buffer IC. The use of LVDS output interface largely eliminates issues with IO supply noise.

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ABSOLUTE MAXIMUM RATINGS

Table 14. Absolute Maximum Ratings (T_A = 25°C, unless otherwise specified).

Parameter	Symbol	Conditions	Min	Max	Units
AVDD	V_{AVDD}	Relative to AVSS	-0.3	2.0	V
DRVDD	V_{DRVDD}	Relative to AVSS	-0.3	2.0	V
VINP, VINM		Relative to AVSS	-0.3	2.0	V
CLK+, CLK-		Relative to AVSS	-0.3	2.0	V
SYNC		Relative to AVSS	-0.3	2.0	V
VCM		Relative to AVSS	-0.3	2.0	V
CSB		Relative to AVSS	-0.3	2.0	V
SCLK		Relative to AVSS	-0.3	2.0	V
SDIO		Relative to AVSS	-0.3	2.0	V
PDWN		Relative to AVSS	-0.3	2.0	V
D0, ..., D11		Relative to AVSS	-0.3	2.0	V
DCO+		Relative to AVSS	-0.3	2.0	V
Operating Temperature Range (Ambient)			-40	85	°C
Maximum Junction Temperature Under Bias				125	
Storage Temperature Range (Ambient)			-65	150	

Notes:

1. Stresses beyond those listed under Table 14 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD CAUTION.

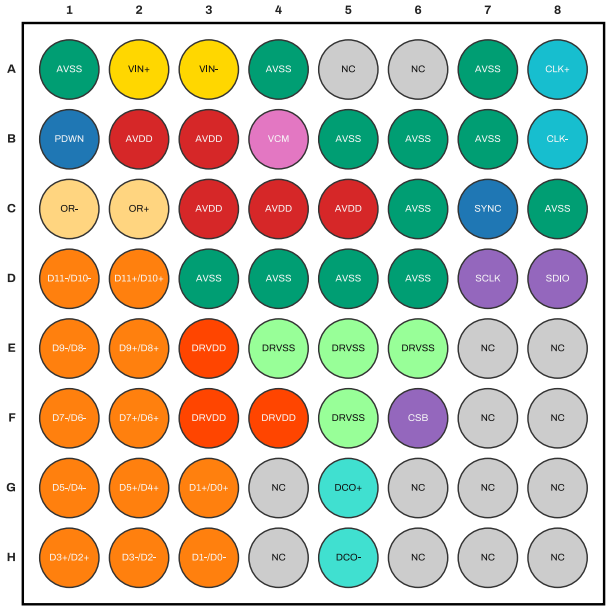


Electrostatic Discharge Sensitive Device.

Proper ESD precautions should be observed to prevent performance degradation or loss of functionality.

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PACKAGE



BGA, size: 3.4mm×3.4mm
Ball pitch: 0.4mm

Figure 5: SD7112 Package Top View for Channel Multiplexed LVDS Configuration.

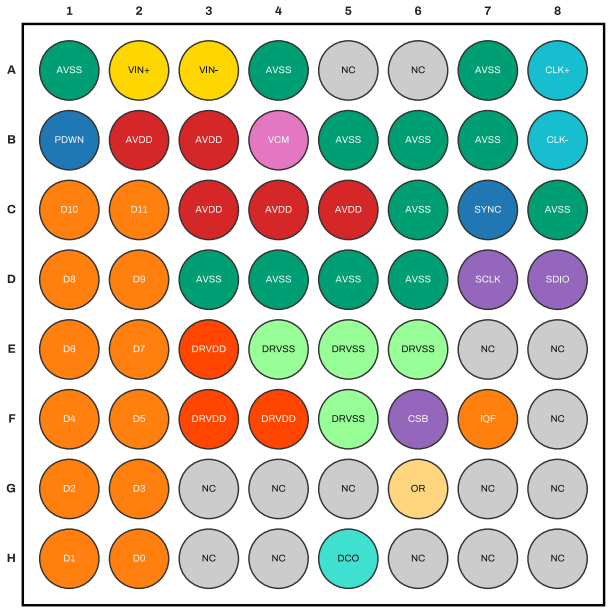
Table 15. Pin Descriptions for Channel Multiplexed LVDS Configuration.

Number	Name	Type	Comment
A1, A4, A7, B5, B6, B7, C6, C8, D3, D4, D5, D6	AVSS	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. The exposed paddle must be connected to ground for proper operation.
A2	VIN+	Input	Differential Analog Input Pin (Plus).
A3	VIN-	Input	Differential Analog Input Pin (Minus).
A5, A6, E7, E8, F7, F8, G4, G6, G7, G8, H4, H6, H7, H8	NC		Do not connect.
A8	CLK+	Input	ADC Clock Input (Plus).
B1	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or stand-by.
B2, B3, C3, C4, C5	AVDD	Power	Analog Power Supply (1.8 V Nominal).
B4	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
B8	CLK-	Input	ADC Clock Input (Minus).
C1	OR-	Output	Channel A/Channel B LVDS Overrange (Minus).
C2	OR+	Output	Channel A/Channel B LVDS Overrange (Plus).
C7	SYNC	Input	Digital Synchronization Pin.

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Number	Name	Type	Comment
D1	D11-/D10-	Output	LVDS Output Data 10 and 11 (Minus).
D2	D11+/D10+	Output	LVDS Output Data 10 and 11 (Plus).
D7	SCLK	Input	Serial interface clock input.
D8	SDIO	InOut	SPI Serial Data I/O.
E1	D9-/D8-	Output	LVDS Output Data 8 and 9 (Minus).
E2	D9+/D8+	Output	LVDS Output Data 8 and 9 (Plus).
E3, F3, F4	DRVDD	Power	Digital I/O Supply.
E4, E5, E6, F5	DRVSS	Ground	Digital I/O Ground.
F1	D7-/D6-	Output	LVDS Output Data 6 and 7 (Minus).
F2	D7+/D6+	Output	LVDS Output Data 6 and 7 (Plus).
F6	CSB	Input	SPI Chip Select (Active Low).
G1	D5-/D4-	Output	LVDS Output Data 4 and 5 (Minus).
G2	D5+/D4+	Output	LVDS Output Data 4 and 5 (Plus).
G3	D1+/D0+	Output	LVDS Output Data 0 and 1 (Plus).
G5	DCO+	Output	LVDS Data Clock Output (Plus).
H1	D3+/D2+	Output	LVDS Output Data 2 and 3 (Plus).
H2	D3-/D2-	Output	LVDS Output Data 2 and 3 (Minus).
H3	D1-/D0-	Output	LVDS Output Data 0 and 1 (Minus).
H5	DCO-	Output	LVDS Data Clock Output (Minus).

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BGA, size: 3.4mm×3.4mm
Ball pitch: 0.4mm

Figure 6: SD7112 Package Top View for Parallel CMOS Configuration.

Table 16. Pin Descriptions for Parallel CMOS Configuration.

Number	Name	Type	Comment
A1, A4, A7, B5, B6, B7, C6, C8, D3, D4, D5, D6	AVSS	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. The exposed paddle must be connected to ground for proper operation.
A2	VIN+	Input	Differential Analog Input Pin (Plus).
A3	VIN-	Input	Differential Analog Input Pin (Minus).
A5, A6, E7, E8, F8, G3, G4, G5, G7, G8, H3, H4, H6, H7, H8	NC		Do not connect.
A8	CLK+	Input	ADC Clock Input (Plus).
B1	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or stand-by.
B2, B3, C3, C4, C5	AVDD	Power	Analog Power Supply (1.8 V Nominal).
B4	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
B8	CLK-	Input	ADC Clock Input (Minus).
C1	D10	Output	CMOS Output Data 10.
C2	D11	Output	CMOS Output Data 11.
C7	SYNC	Input	Digital Synchronization Pin.
D1	D8	Output	CMOS Output Data 8.

Number	Name	Type	Comment
D2	D9	Output	CMOS Output Data 9.
D7	SCLK	Input	Serial interface clock input.
D8	SDIO	InOut	SPI Serial Data I/O.
E1	D6	Output	CMOS Output Data 6.
E2	D7	Output	CMOS Output Data 7.
E3, F3, F4	DRVDD	Power	Digital I/O Supply.
E4, E5, E6, F5	DRVSS	Ground	Digital I/O Ground.
F1	D4	Output	CMOS Output Data 4.
F2	D5	Output	CMOS Output Data 5.
F6	CSB	Input	SPI Chip Select (Active Low).
F7	IQF	Output	IQ Channel Indicator or Flag.
G1	D2	Output	CMOS Output Data 2.
G2	D3	Output	CMOS Output Data 3.
G6	OR	Output	Overrange Output.
H1	D1	Output	CMOS Output Data 1.
H2	D0	Output	CMOS Output Data 0.
H5	DCO	Output	Clock Output.

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TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 80MHz, A_{IN} = -1dBFS, differential AC-coupled clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

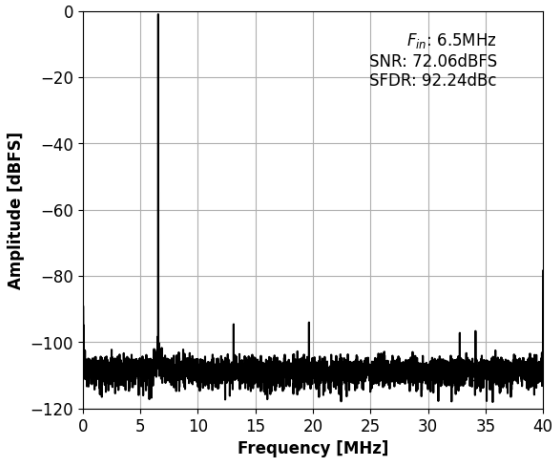


Figure 7: Single-Tone FFT with f_{IN}=6.55MHz.

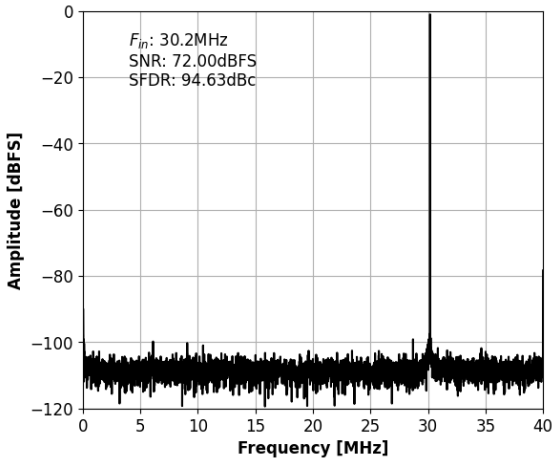


Figure 8: Single-Tone FFT with f_{IN}=30.2MHz.

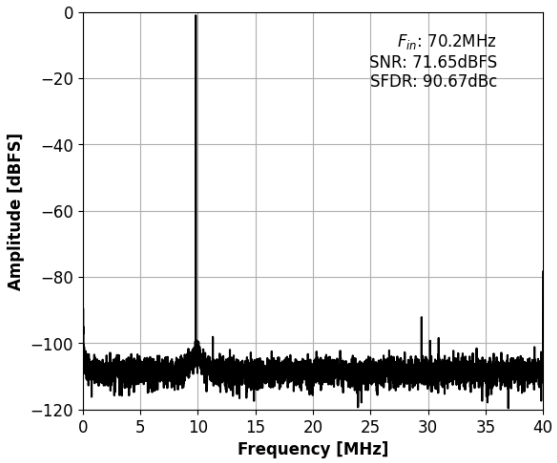


Figure 9: Single-Tone FFT with f_{IN}=70.2MHz.

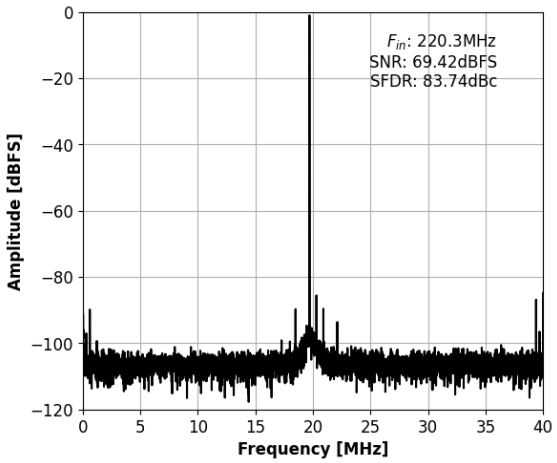


Figure 10: Single-Tone FFT with f_{IN}=220MHz.

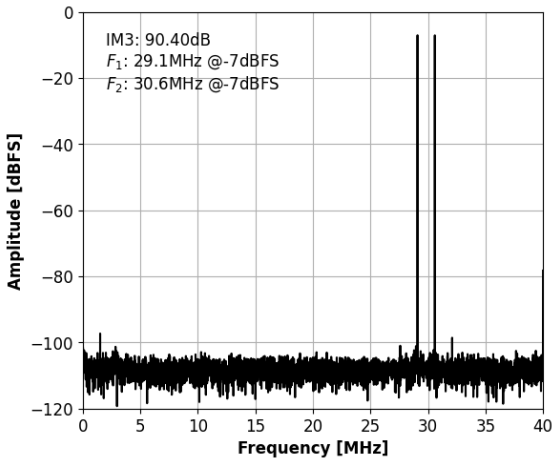


Figure 11: Two-Tone FFT with f_{IN1}=29.1MHz, f_{IN2}=30.6MHz.

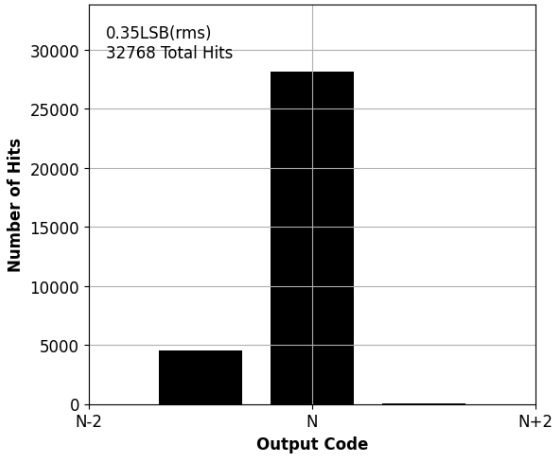


Figure 12: Grounded Input Histogram.

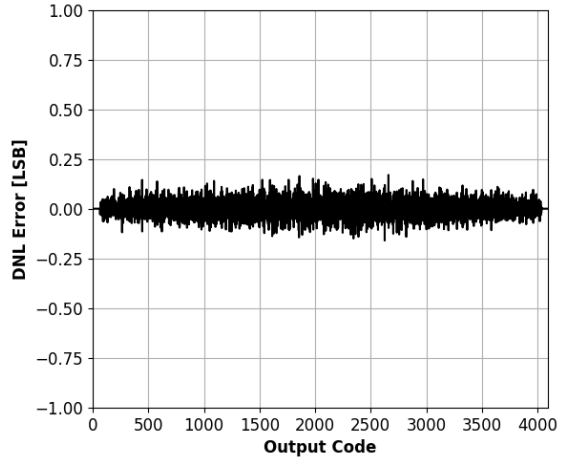


Figure 13: DNL Error with f_{IN}=6.55MHz.

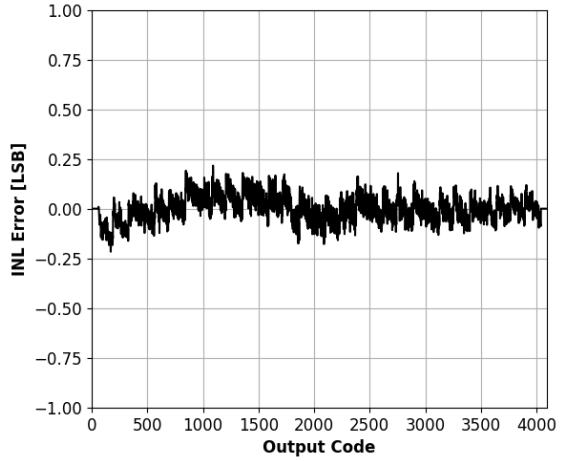


Figure 14: INL Error with f_{IN}=6.55MHz.

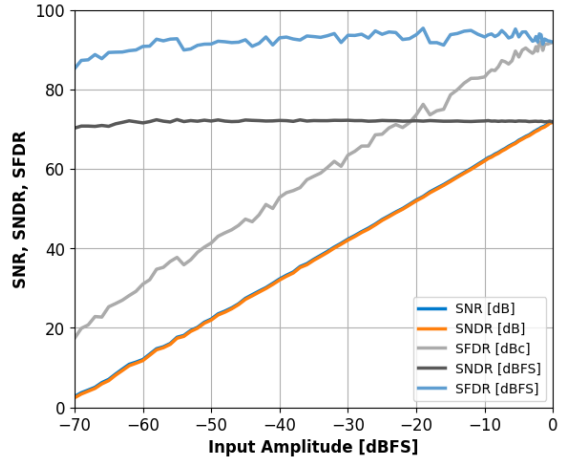


Figure 15: Single-Tone SNR, SNDR and SFDR vs. Input Amplitude with f_{IN}=30.25MHz.

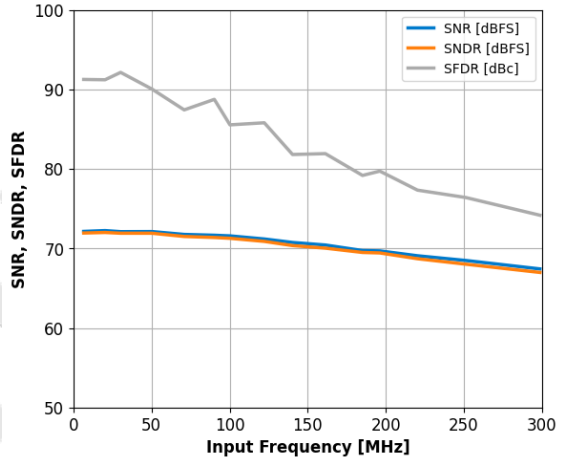


Figure 16: Single-Tone SNR, SNDR and SFDR vs. Input Frequency with f_S=80MHz.

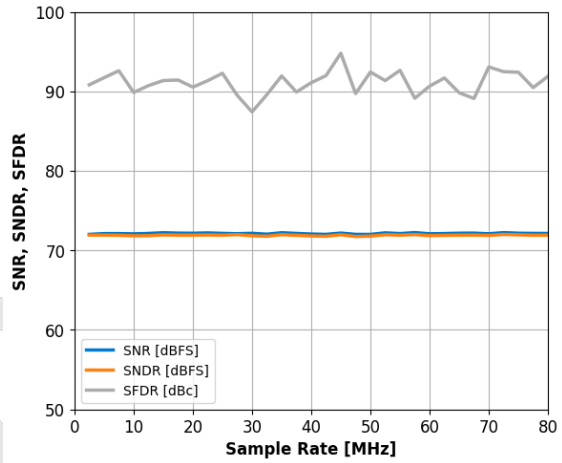


Figure 17: Single-Tone SNR, SNDR and SFDR vs. Sample Rate with f_{IN}=30.25MHz.

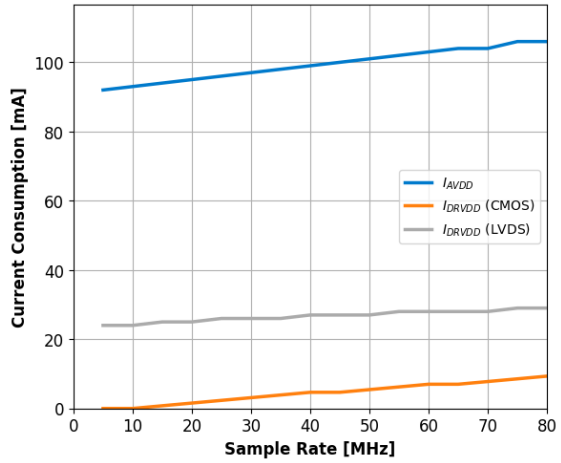


Figure 18: Current vs. Sample Rate.

EQUIVALENT CIRCUITS

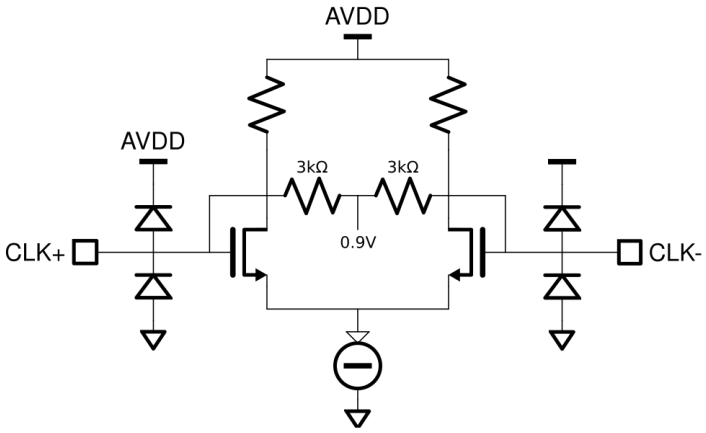


Figure 19: Equivalent Clock Input Circuit.

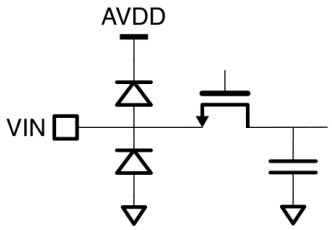


Figure 20: Equivalent Analog Input Circuit.

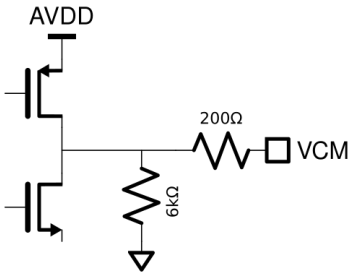


Figure 21: Equivalent VCM Circuit.

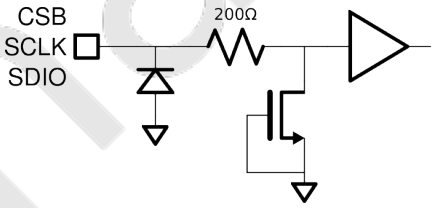


Figure 22: Equivalent CSB, SCLK/DFS, SDIO/PDWN or MODE Input Circuit.

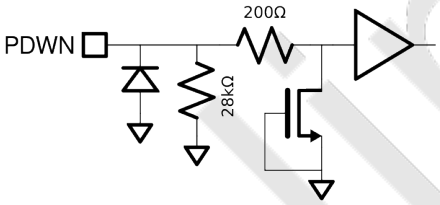


Figure 23: Equivalent PDWN Input Circuit.

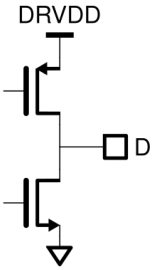


Figure 24: Equivalent Digital Output Circuit.

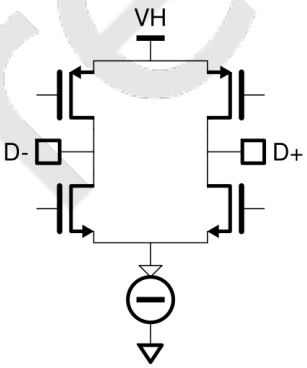


Figure 25: Equivalent LVDS output Circuit.

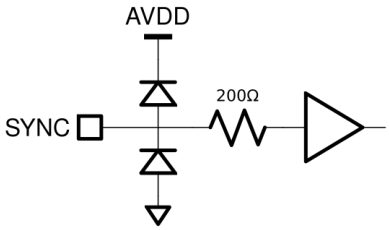


Figure 26: Equivalent SYNC Input Circuit.

Preliminary

THEORY OF OPERATION

ADC Architecture

The ADC uses a pipelined architecture and innovative patented switched-capacitor circuits. Its fully differential design provides exceptional immunity to power supply noise and minimizes reference voltage self-modulation. A built-in Sample-and-Hold (S/H) function is integrated into the input stage of the pipeline structure.

Analog Input

The input stage of the ADC behaves as a switched-capacitor network, presenting itself to the driving circuit as a combination of a switch and a sampling capacitor. The capacitor is reset prior to each conversion cycle, effectively eliminating non-linear memory effects commonly observed in some pipelined ADC architectures. The ADC does not include an internal common-mode bias therefore, the driving source must provide an appropiate common-mode voltage.

Differential Clock Input

The SD7112 features a differential clock receiver with an integrated common-mode bias. For proper operation, the clock inputs should be AC-coupled using 10nF capacitors.

Differential Clock Configuration. For optimal jitter performance, a differential clock source is recommended. The differential clock signals to CLK+ and CLK- should be connected through a 10nF AC-coupling capacitors.

Single-Ended Clock Configuration. If a single-ended clock source is used, the signal source should be AC-coupled to the CLK+ pin. In this configuration, a 10nF capacitor should be connected between the CLK- pin and analog ground to maintain proper biasing.

Clock Jitter Considerations. Clock jitter has a significant impact on the ADC's signal-to-noise ratio (SNR). The sensitivity to jitter increases with input signal frequency. For best performance, a low-noise differential clock with fast edge transitions should be used.

Note: The part can enter in manufacturing test mode if both differential clock inputs are held low for more than 1ms. This behavior can be prevented by writing 1 to register *0x4cf*, bit[15].

Clock Divider

The ADC includes a programmable clock divider that allows the input clock to be divided by integer values from 2 to 8. The divider is configured by setting register *0x463*, bits [7:5], to the desired division value. A value of 0 (default) bypasses the divider entirely.

By default, the divider starts asynchronously. If the application requires synchronization across multiple ADC devices, the SYNC pin provides means for aligning clock dividers to guarantee sampling on the same clock edge. If clock divider is bypassed, this feature is not needed.

Synchronization is enabled by setting register *0x463*, bit [10], to 1. When the bit is 0, SYNC pin is ignored. SYNC is a level sensitive, active high, reset pin that is captured on the falling edge of the input clock. As long as SYNC is high, the divider stays in reset. It starts dividing on the first falling clock edge after SYNC goes low.

Make sure that the falling edge of SYNC meets the specified setup and hold times relative to the input clock, as shown in Table 12. Pay attention to the length matching of the clock and SYNC routing to the multiple ADC chips. For test and debugging purposes, the level of received and captured SYNC signal can be read from register *0x4ff*, bit [10].

Clock Duty-Cycle Requirements. The ADC utilizes both the rising and falling edges of the input clock (or the divided clock, if the divider is enabled) for internal sampling operations. To achieve optimal performance, especially at the maximum sampling rate, the clock duty cycle should be as close to 50% as possible.

When the divider is enabled with an even divisor, a 50% duty cycle is guaranteed by design. If the application uses a clock with a non-ideal duty cycle, a Duty Cycle Stabilizer (DCS) can be enabled to improve performance.

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ADC Self-Calibration

The ADC includes an automatic calibration mechanism that is executed at power-up to ensure optimal performance. It calibrates out capacitor mismatch and the effects of operational amplifier finite gain and bandwidth. For best results, calibration should be performed at the actual sampling rate used during operation. To support this, the device continuously monitors the sampling clock frequency and automatically re-triggers calibration if a significant change is detected. This feature can be disabled by setting register *0x4c9*, bit[0], to 1.

Manual calibration can also be initiated by toggling from 0 to 1. The calibration process is implemented using a state-machine architecture, ensuring a deterministic and predictable calibration time. By default the calibration takes 46 million ADC sampling clock cycles. Calibration completion status can be read from after the status readback is enabled by writing 0x1c to Bit value 1 indicates that calibration is complete.

In addition, the ADC supports a Background Calibration (BGC) mode, which is disabled by default. When enabled, parameters for compensating changes in operational amplifier gain and bandwidth are continuously updated. BGC is beneficial in environments with large temperature variations near the hot end of the specified operating temperature range. For its operation, BGC uses a dither signal which is injected into the ADC input signal path. This dither consumes approximately 0.8dB of the ADC's input range, resulting in earlier clipping compared to when BGC is disabled. When BGC is enabled calibration completion status bit remains 0.

To enable BGC:

- Write 0b01 to register 0xde1, bits [15:14]
- Write 0b0 to register 0xde3, bit [3]
- Write 0x0d80 to register 0xdcf

Calibration parameters can be altered to optimize ADC performance and the duration of the calibration according to Table 17.

High Performance settings improve the low frequency SFDR compared to the default settings while the High Speed Settings minimize the calibration time at the cost of small SFDR and SNDR degradation. If the parameters are altered, the calibration has to be reinitiated as described earlier.

Table 17. Calibration Settings.

Register Address	Default Value	High Performance Value	High Speed Value
0xdcd	*0x1483*	*0x3483*	*0x348c*
0xdd5	*0x1483*	*0x3483*	*0x348c*
0xddd	*0x16c3*	*0x36c3*	*0x36cc*
0xde1	*0xbbe8*	*0xbb80*	*0xbb20*
Duration (clock cycles)	46M	25M	6.3M

Stand-by and Power-Down Modes

The SD7112 supports two power-saving modes, power down and stand-by, that can be used when the ADC is not actively sampling. In both modes, the SPI interface (if enabled) remains operational.

Power-Down Mode. This mode disables most of the internal circuitry, resulting in the lowest residual supply current. It is ideal for applications requiring minimal power consumption during idle periods. Power-down mode can be enabled via either of the following:

- The PDWN pin, or
- Setting register *0x457*, bit[7], to 1.

Stand-by Mode. Stand-by mode offers a faster wake-up time compared to power-down mode, at the cost of slightly higher residual current. It is suitable for applications that require rapid recovery from idle states. To enable stand-by mode, set register *0x457*, bits [3] and [8], to 1.

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Note: It is recommended to disable the ADC auto-calibration when using stand-by mode to avoid unintended calibration cycles during transitions.

Commonly Used Functions

The SD7112 offers several functions available via dual function pin controls (external pin mode vs. SPI mode). The SD7112 detects the SPI mode during the first SPI transaction after power-up. If the user does not want to program the device via the SPI interface, the dual function is available.

Duty-Cycle Stabilizer. The Duty-Cycle Stabilizer (DCS) retimes the falling edge of the clock thus providing an internal clock signal with a 50% duty cycle. The DCS is useful in systems where the input clock has an uneven duty cycle. It can be enabled via register control, by setting register *0x457*, bit[1], to 1.

Output Enable (active-low, **OEB**). The output data drivers can be placed in a high-impedance state using the OEB function, accessed by setting register *0x457*, bit[3], to 1.

Common-Mode Voltage. The VCM pin outputs the analog input common-mode bias voltage (VCM). This pin provides a stable DC reference that can be used to set the ADC input common-mode level, either directly through a passive network or indirectly as the common-mode reference for a driving amplifier. In typical applications, the default common-mode voltage is suitable and requires no adjustment. The common-mode voltage level is programmable through register *0xf11*, bits [4:3].

Overrange Indicator. This output bit indicates that the analog input sample exceeded the converter's full-scale input range. When the input signal exceeds the converter's positive (or negative) full-scale range, the ADC will clip, and the output data will saturate to the maximum (or minimum) digital code. In either case, the OR bit will be set, indicating that the input had been out of range during that sample.

Internal Reference Voltage

The internal vref can be adjusted with *0x45d* bits [4:1]. Usually, the default value yields the optimal performance.

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DSP

The DSP path, shown in Figure 27, includes functionality for processing the output data of two ADCs operated as an IQ pair or independently. All functions can be bypassed or disabled if not needed. The main blocks in the signal chain are input multiplexer, sample delay control, gain and offset correction, phase correction, digital down converter (DDC), and decimator. Refer to APP-NOTE 100 (*Understanding the DSP Features in Plural™ Family of ADCs*) for more details on this topic.

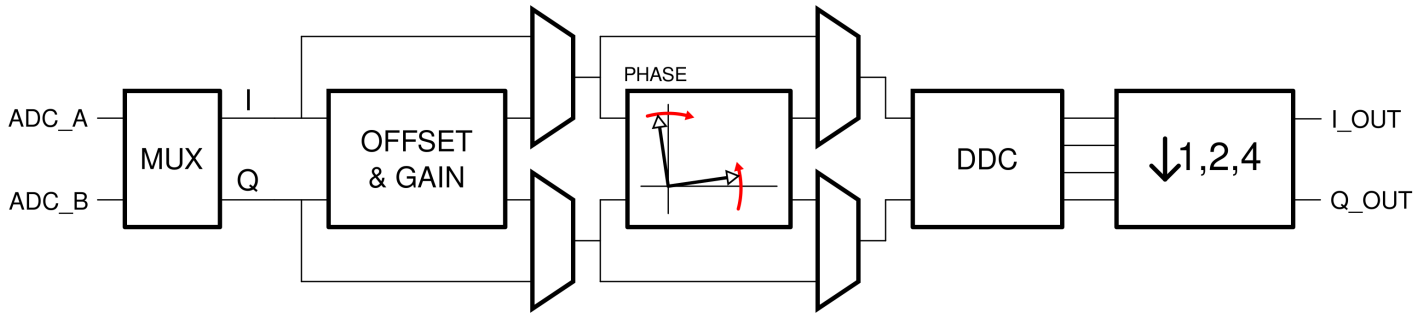


Figure 27: SD7112 DSP Top-Level Diagram.

Input MUX

The DSP block has two inputs, both with a multiplexer for selecting the source signal. By default ADC B feeds the I (in-phase) input and ADC A the Q (quadrature) input. The MUX allows crossing the inputs, feeding the same ADC to both inputs, and using the average of the two ADC outputs as a source. The multiplexer is controlled by register *0xf09*.

Delay, Offset, and Gain

Datapath configiration and sample delay control bits are in register *0x807*. Gain and offset are controlled by registers *0x809*, *0x80b*, *0x80d*, and *0x80f*.

IQ Phase Correction

The block diagram of IQ phase correction block is shown in Figure 28. It can be used to add or subtract a small amount of I signal form the Q and vice versa to compensate for the phase error of the input signal. The correction range is about ±14 degrees and it is controlled by the *0x811* register. This simple scheme affects both the signal phase and gain and thus has to be used together with the gain correction block to minimize both the gain and phase mismatch.

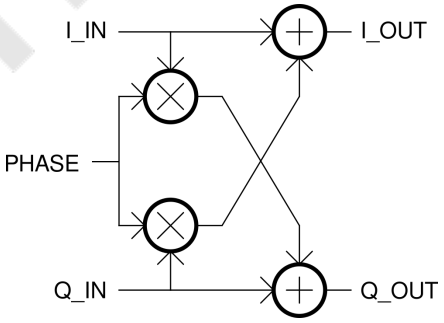


Figure 28: SD7112 IQ phase correction.

Digital Down Converter (DDC)

Figure 29 shows the block diagram the DDC. It consists of two numerically controlled oscillators (NCOs), digital multipliers, adders, and multiplexers. It can be programmed for two modes of operation. Mode 1 provides two independent paths with a real input and a complex (IQ) output. Mode 2 is used when the two ADCs operate as an IQ pair. It accepts IQ input and

supplies IQ output using NCO1 as local oscillator (LO).

The DDC is enabled in the datapath using a bit in register *0x807*. Its control bits are collected in register *0x813*, which has bits for enabling the I and Q paths and selecting the NCOs. The mode is selected using bits [14:13], value 0b01 selecting mode 1 and value 0b10 mode 2. In mode 2 the spectral inversion can be done by manipulating the signs of the adder inputs using bits [11:8], value 0b1101 is the default and value 0b0001 inverts the frequency axis.

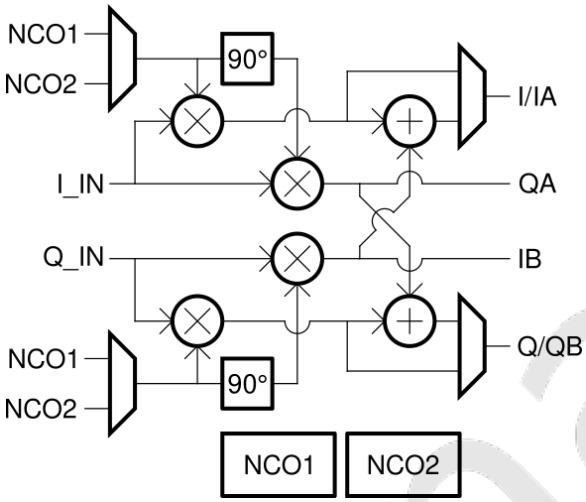


Figure 29: SD7112 DDC.

NCO

The two NCO instances are implemented using a direct digital synthesizer (DDS). It can produce a LO frequency ranging from 0 to F_s using a 48-bit frequency control word, which is calculated as f/F_s*2^{48}. To program the frequency, the DDC must be first enabled and a stable input clock must be present. Registers *0x815*, *0x817*, and *0x819* control NCO1 and registers *0x81b*, *0x81d*, and *0x81f* control NCO2. After the new frequency is written to the registers it has to be loaded by setting load bit high and then clearing it. NCO1 uses bit [0] and NCO2 bit [1] in register *0x82b* for this purpose.

Decimator

The final block in the DSP signal chain is the decimator, which supports rates 2 and 4 or can be bypassed. It is based on two cascaded half-band FIR filters with the frequency response shown in Figure 30. The operation of the decimator is controlled by three registers *0x82f*, *0x82d*, and *0x805* that configure the decimator, set the rate, and DSP output clock divider.

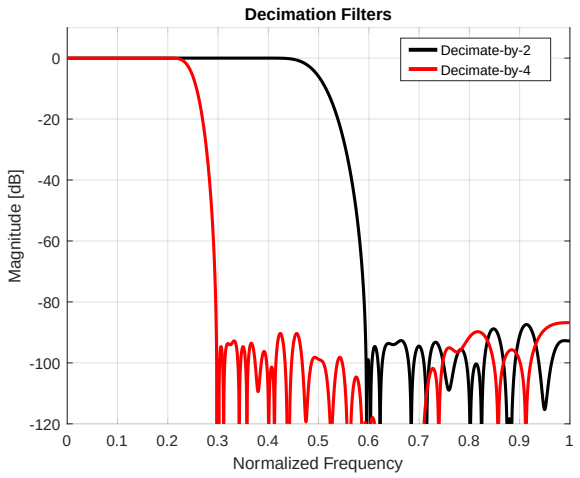


Figure 30: SD7112 Decimator Frequency Response.

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Table 18 provides the register values for each mode of operation.

Table 18. Decimation Modes.

Mode	DSP Output Clock Rate	Reg *0x82f*	Reg *0x82d*	Reg *0x805*
Bypass	1	0x0001	0x0000	0x0000
Decimate by 2	1/2	0x0006	0x0010	0x0001
Decimate by 4	1/4	0x0026	0x0020	0x0002
DDC mode 1 & Decimate by 2	1	0x000E	0x0010	0x0000
DDC mode 1 & Decimate by 4	1/2	0x002E	0x0020	0x0001
Interleave & Decimate by 2	1/2	0x0016	0x0000	0x0000
Interleave & Decimate by 4	1/4	0x0032	0x0010	0x0001

Interleave and Decimate Mode

To operate the two ADC cores as an interleaved unit the input clock must be provided at twice the core sampling rate. The decimator is programmed per Table 18 and the ADCs are configured for interleaving using the following steps, which can only be performed after a stable input clock is present. Interleaving without decimation is not supported.

1. Write 0x0022 to register *0xf0f* to enable clock division by two.
2. Write 0x0000 to register *[ADC_B_ADC_CORE_CLK_CTRL_register]* and 0x0002 to register *0xdc3* to set the clocks of the two ADC cores 180 degrees apart.
3. Toggle clock divider reset bit by first writing 0x0003 and then 0x0043 to register *0xf07*.
4. Program digital logic to work with 180 degree sampling clock offset by writing 0x000C to register *0xde7*.

In this mode the digital output data is present on both ADC A and ADC B output pins. The redundant output pins can be turned off to save power and reduce IO noise.

Down Mixing Before Decimation

When decimating by two, the signals located in the upper half of the first Nyquist zone fall into the stop band of the decimation filter. Similarly the decimate by four mode passes signals up to $0.1F_s$ while blocking them from there on up to $0.9F_s$. The DDC block has a low power mode that uses a simple sequence of +1 and -1 multiplications that can mix the signal down with LO at $F_s/2$ or $F_s/4$ before decimation. This is enabled by the following steps, which can be exececuted only after a stable input clock is present.

1. Enable DDC in the datapath by clearing register *0x807* bit[9].
2. Write 0x59AB for LO of $F_s/2$ and 0x392B for LO at $F_s/4$ to register *0x813*.
3. Load the LO frequency by first writing 0x0001 and then 0x0000 to register *0x82b*.
4. Enable DDC low power mode by writing 0x59EB for LO of $F_s/2$ and 0x396B for LO of $F_s/4$ to register *0x813*.

An alternative and more versatile way to mix the signal down before decimation is to use the DDC. One significant difference is the digital output in IQ format.

In interleave and decimate mode, programming the part for mixing down with $F_s/4$ is the same as mixing down with $F_s/2$ above, as the definition of F_s has changed by a factor of two. Setting the LO at $F_s/2$, which means multiplying every other sample by +1 and every other by -1, can be accomplished in two ways: in the board level by crossing the + and - of the analog input of one of the converters or using the following steps.

1. Enable DDC in the datapath by clearing register *0x807* bit [9].
2. Write 0x58AB to register *0x813*.
3. Set register *0x807* bit [0].
4. Load the LO frequency by first writing 0x0001 and then 0x0000 to register *0x82b*.
5. Clear register *0x807* bit [0].

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6. Enable DDC low power mode by writing 0x58EB to register *0x813*.

Digital IOs

When the DSP is enabled the I-output is mapped to the ADC B output pins and the Q-output is mapped to the ADC A output pins. The rate of the digital output clock relative to the sampling clock (input clock after the clock divider) is specified in Table 18.

When the DDC is programmed to mode 1, it produces two IQ output signals each of which is interleaved into the corresponding ADC's output pins sending out the I and Q samples on alternate clock cycles. This output mode is enabled by writing 0b01 to register *0x4b5*, bits [10:9]. The ADC B overrange pin can be programmed to serve as IQ indicator that toggles on every output clock cycle, by setting register *0x4cd*, bit [7]. A high value indicates a Q sample in A output and I sample in B output.

This mode suffers from a startup condition that instead of pairing sample Q(n) with sample I(n), sometimes Q(n) sample is paired with sample I(n-1) or I(n+1). Which of the two states is active can be detected with the following procedure and then handled properly in the receiver.

1. Program DSP to the desired mode of operation.
   a. If decimating by 2, program the DDS to frequency 0x200000000000
   b. if decimating by 4, program the DDS to frequency 0x100000000000
2. Load the frequency as described earlier (this creates a deterministic digital test pattern).
3. Set DDC output mux (register *0x813*, bits [14:13]) to 0b11 to enable the test pattern.
4. Observe the MSB of the received digital signal de-interleved into I and Q. Correct pairing shows the MSB of the Q-channel leading the I-channel by one sample. The correct state can be identified by delaying the MSB of Q and comparing it to the MSB of I. If any bit in the four-sample-long test pattern shows a mismatch, the samples are paired incorrectly. They should be realigned by applying a one-sample delay to Q of the B output and I of the A output in the receiver. The detection can be made with a simple XOR based circuit (see Listing 1).
5. Restore DDC output mux value to 0b01 and program the DDS(s) to the desired LO frequency.

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Listing 1: The IQ-alignment SystemVerilog Module.

```
module iq_align (
   input  logic clk,               // clock
   input  logic [15:0] da, db,     // 16-bit input data streams
   input  logic orb,               // Channel B overrange bit. Its second function identifies
                                   // whether the current data belongs to Q or I
   input  logic sel,               // Select between da and db, for alignment check
   input  logic align_now,         // Pulse to perform alingment. Must be minimum 4 clocks long
   input  logic capture_iq_flag,   // Pulse to capture orb
   input  logic reset_delay,       // Reset delay to 0
   output logic [15:0] da_i, da_q, // I/Q components of channel A
   output logic [15:0] db_i, db_q  // I/Q components of channel B
);
   // Synchronize locally generated I/Q indicator (iq_flag) to the one provided by
   // the chip on 'orb' pin.
   logic iq_flag;
   always_ff @(posedge clk)
      iq_flag <= ~(capture_iq_flag ? orb : iq_flag);

   // Split the input data into I and Q streams
   logic [15:0] da_i0, db_i0, da_q0, db_q0, da_i1, db_q1;
   always_ff @(posedge clk) begin
      if (iq_flag) begin
         da_i0 <= da; // High flag indicates I on channel A
         db_q0 <= db; // High flag indicates Q on channel B
      end else begin
         da_q0 <= da;
         db_i0 <= db;
         da_i1 <= da_i0;
         db_q1 <= db_q0;
      end
   end

   // Output data is launched on every other clock cycle, applying a delay to da_i and db_q
   // when misalignment is detected
   logic da_q_d_15, db_q_d_15, delay;
   always_ff @(posedge clk)
      if (~iq_flag) begin
         da_q <= da_q0;
         da_i <= delay ? da_i1 : da_i0;
         da_q_d_15 <= da_q[15];
         db_i <= db_i0;
         db_q <= delay ? db_q1 : db_q0;
         db_q_d_15 <= db_q[15];
      end

   // Compare the MSB of I and delayed Q to detect misalignment.
   // When the alingment is correct, the the signals are identical.
   wire misaligned = sel ? da_i[15]^da_q_d_15 : db_i[15]^db_q_d_15;

   // Enable delay, if misalignment is detected.
   always_ff @(posedge clk)
      if (reset_delay)
         delay <= 1'b0;
      else if (align_now & misaligned)
         delay <= 1'b1;
endmodule
```

Listing 1 shows an example SystemVerilog implementation of the alignment detection and correction logic. This implementation is provided as a reference and may require adjustments to meet specific customer requirements.

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SERIAL PORT INTERFACE

The SD7112 uses a 3-wire Serial Port Interface (SPI) that gives the user flexibility to configure the converter for specific functions, depending on the application, through a register space provided inside the ADC. The interface signals are:

- SCLK: defines the bit rate at which serial data is driven onto, and sampled from, the bus;
- CSB: defines the boundaries of a basic data 'unit', comprised of multiple serial bits;
- SDIO: is the serial data IO wire;

The read and write cycles are described in the figure below. The address space is 13 bits long (A<12:0>) and the data is 16 bits wide (D<15:0>). The complete instruction cycle is 32-bits long. The falling edge of CSB combines with the rising edge of SCLK marks the start of the instruction cycle. On a write transaction, the target register is updated on the falling edge of SCLK.

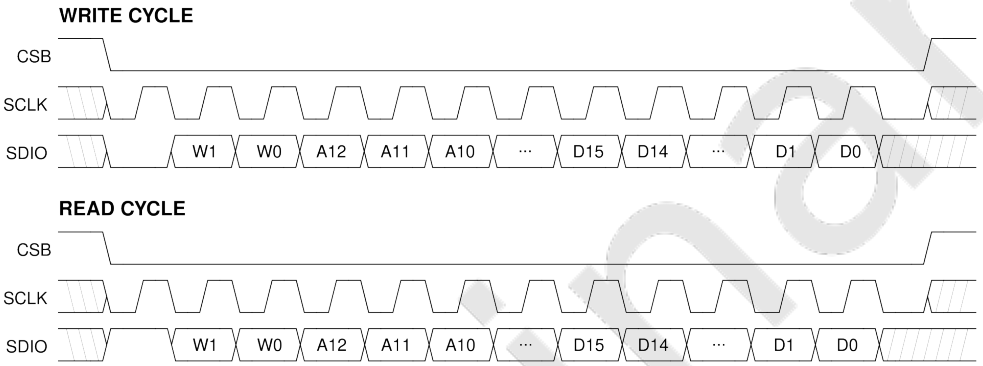


Figure 31: 3-wire SPI timing.

Table 19. SPI Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Setup time between the data and the rising edge of SCLK	t_{DS}	2			ns
Hold time between the data and the rising edge of SCLK	t_{HD}	2			ns
Period of the SCLK	t_{SCLK}	40			ns
Setup time between CSB and SCLK	$t_{S,CSB-SCLK}$	2			ns
Hold time between CSB and SCLK	$t_{H,CSB-SCLK}$	2			ns
Minimum period that SCLK should be in a logic high state	$t_{SCLK,high}$	10			ns
Minimum period that SCLK should be in a logic high state	$t_{SCLK,low}$	10			ns
Time from SCLK falling edge to SDIO switching from input to output	$t_{SDIO,EN}$	10			ns
Time from SCLK falling edge to SDIO switching from output to input	$t_{SDIO,DIS}$	10			ns

Two bits, W1 and W0, determine how many bytes of data that can be transferred in the same write cycle (see Table 20). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.

Table 20. SPI Word Length.

[W1,W0]	Data length
00	Not supported
01	Two bytes of data can be transferred
10	Not supported
11	Four bytes of data can be transferred

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The SPI pins should not be active when the full dynamic performance of the ADC is required. Noise from SCLK, CSB and the data transactions can degrade ADC performance.

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OUTPUT MODE

Data Scrambler

Interference originating from the digital outputs of the ADC can be difficult to eliminate entirely. Such interference may result from capacitive or inductive coupling mechanisms, or from shared impedance paths in the ground plane. Even minimal coupling coefficients can introduce deterministic spurious tones into the ADC's output frequency spectrum. To mitigate this, digital output scrambling techniques can be employed prior to off-chip transmission. By randomizing the bit patterns, the spectral energy of these spurs is dispersed, effectively reducing their peak amplitudes and minimizing their impact on signal integrity.

The SD7112 can apply an exclusive-OR logic operation between the LSB and all other data output bits, while the LSB, overflow and clock outputs are not affected.

When this function is used, the receiver must apply the same function to unscramble the received data.

The data scrambler is enabled by setting control register *0x4b5*, bit[13], to 1.

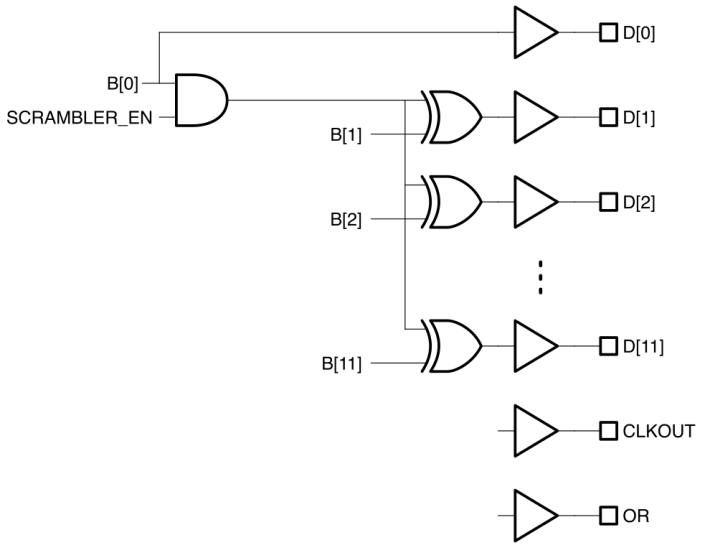


Figure 32: SD7112 Data Scrambler.

Alternate Bit Polarity

The alternate bit polarity is particularly effective to suppress digital feedback and minimize noise coupling on the PCB when the ADC input signal is near mid-scale and of very small amplitude. In this case, the digital output tends to toggle between patterns dominated by either logic high or logic low states. This synchronized switching of multiple bits can induce significant transient currents in the ground plane, leading to increased digital noise. This mode, when activated, inverts all odd-numbered data output bits prior to the output buffer stage while even-numbered bits, along with the overflow and clock output, remain unaffected thus ensuring that approximately half of the output bits transition are high while the other half transition are low. This balanced switching behavior helps cancel out opposing current flows in the ground return path, thereby reducing overall ground noise. At the receiving end, the original data can be reconstructed by inverting the same odd-numbered bits. This mode operates independently of the digital output randomization feature, both functions can be enabled or disabled separately. The Alternate Bit Polarity mode is configured via serial programming of control register *0x4b5*, bit[14].

Output Test Modes

The output test options are described in Table 21 and are selected via SPI programming at register *0x4b5*, bits [5:2].

When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. These tests require an active input clock.

There are two pseudo-random number generators available, PN23 and PN9. The PN23 generator ($X^{23}+X^{18}+1$), selected by register *0x4b5*, bits [5:2], set to 0x5, can be reset by setting register *0x4b5*, bit [12], low; while the PN9 generator ($X^{9}+X^{5}+1$), selected by register *0x4b5* set to 0x6, can be reset by setting register *0x4b5*, bit [11], low.

Table 21. Output Test Modes.

Mode	Function
0	Pass-Through
1	Midscale
2	+FS
3	-FS
4	Checkerboard
5	PN23
6	PN9
7	1/0 word toggle
8	User input
9	1/0 bit toggle
10	Unused
11	1-bit high
12	Mixed frequency
13	Unused
14	Unused
15	Ramp

Pass-through and test patterns 1, 2, 3, 5 and 6 are subject to output formatting, while the other test modes are not. Test patterns 1 to 8 and 15 can be applied to using *0x4b5*, bit[7:6]. Patterns 4 and 7 can be toggled between the pattern and its inverse while test pattern 8 can be selected using registers *0x4bb* and *0x4bd*.

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CONTROL REGISTERS

This section describes the most commonly used control registers. For a description of the complete register map, refer to Appendix A: Register Map.

Each register is presented in the following format:

Address: <HEX value>		**RW** or **RO**	**Default: <HEX value>**
bit field	default value	field description.	

Notes

- **RW** = Read/Write
- **RO** = Read-Only
- For read-only registers, the default value is omitted.
- Registers not listed in these tables should not be written.



When updating control register values, always use a read-modify-write procedure. Some registers include reserved bit fields for internal engineering purposes. This approach ensures that these reserved bits remain unchanged and prevents unintended modifications.

CHIP TOP:

Address: 0x457		**RW**	**Default: 0x0015**
[0]	0x1	Duty Cycle Stabilizer enable (see Duty-Cycle Stabilizer). 0: Disable 1: Enable	
[1]	0x0	Duty Cycle Stabilizer on/off in SPI mode (see Duty-Cycle Stabilizer). 0: Off 1: On	
[2]	0x1	Reserved.	
[3]	0x0	Output disable (see Output Enable). 0: Output enabled 1: Output in high-impedance mode.	
[6:4]	0x1	Reserved.	
[7]	0x0	Software power down. 0: Active State 1: Power Down	
[8]	0x0	Software stand-by mode. 0: Active State 1: Stand-by Mode	

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Address: 0x463		RW	Default: 0x0019
[0]	0x1	Enable clock receiver. 0: Disable 1: Enable	
[4:1]	0xc	Reserved.	
[7:5]	0x0	Clock RX divider control. 0: Bypass 1: Divide by 2 2: Divide by 3 3: Divide by 4 4: Divide by 5 5: Divide by 6 6: Divide by 7 7: Divide by 8	
[8]	0x0	Enable on-chip 100Ohm termination. 0: Disable 1: Enable	
[9]	0x0	Clock polarity control when DCS is enabled. 0: Disable 1: Invert	
[10]	0x0	Enable SYNC pin synchronization. 0: Disable 1: Enable	

Address: 0x465		RW	Default: 0x0001
[2:0]	0x1	Output data interleaver. 0-5: N/A 6: even-odd interleaving 7: odd-even interleaving	

Address: 0x473		RW	Default: 0x0000
[4:0]	0x0	Reserved.	
[8:5]	0x0	Output data delay in parallel CMOS mode. The output data delay (250ps steps) with respect to the clock	
[9]	0x0	Launching output clock polarity in parallel CMOS mode. 0: Not inverted 1: Inverted	
[13:10]	0x0	Output clock delay. The output clock delay is increased by 250ps * (register value) with respect to the data	
[14]	0x0	Output clock polarity. 0: Not inverted 1: Inverted	

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Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0	Output format. 0: Offset binary 1: Two's complement 2: Gray code 3: Offset binary	
[5:2]	0x0	Output test mode select (see Table 21).	
[6]	0x1	Output test channel. 0: Disable 1: Enable	
[7]	0x1	Reserved.	
[8]	0x0	Output test toggle mode. Toggle between user test pattern 0 and 1.	
[10:9]	0x0	Reserved.	
[11]	0x1	PN9 generator reset (active low).	
[12]	0x1	PN23 generator reset (active low).	
[13]	0x0	Enable the output data scrambler. 0: Disable 1: Enable	
[14]	0x0	Enable alternate bit polarity switch. 0: Disable 1: Enable	

ADC:

Address: 0xdc1		RW	Default: 0xbfff
[3:0]	0xf	Reserved.	
[4]	0x1	Calibration soft reset (active low).	
[15:5]	0x5f9	Reserved.	

See Table 17 for valid configurations for the following registers:

Address: 0xdcd		RW	Default: 0x1483
[2:0]	0x3	Stg1 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stg1 calibration randomization sequence in foreground mode (see Table 17).	

Address: 0xdd5		RW	Default: 0x1483
[2:0]	0x3	Stage 2 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stage 2 calibration randomization sequence in foreground mode (see Table 17).	

Address: 0xddd		RW	Default: 0x16c3
[2:0]	0x3	Stage 3 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0xd8	Reserved.	
[13:12]	0x1	Stage 3 calibration randomization sequence in foreground mode (see Table 17).	

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Address: 0xde1		RW	Default: 0xbae8
[7:0]	0xe8	Time allocated for calibration (see Table 17).	
[8]	0x0	Enable calibration (see Table 17).	
[9]	0x1	Enable foreground calibration (see Table 17).	
[10]	0x0	Reserved.	
[11]	0x1	Enable stg1 calibration (see Table 17).	
[12]	0x1	Enable stage 2 calibration (see Table 17).	
[13]	0x1	Enable stage 3 calibration (see Table 17).	
[14]	0x0	Background calibration parallel mode (see Table 17).	
[15]	0x1	Disable background calibration mode for all stages (see Table 17).	

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ADC BRING-UP

The SD7112 does not require a specific power-up sequence; however, it is recommended to apply the DRVDD first followed by the AVDD.

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PACKAGE DRAWING

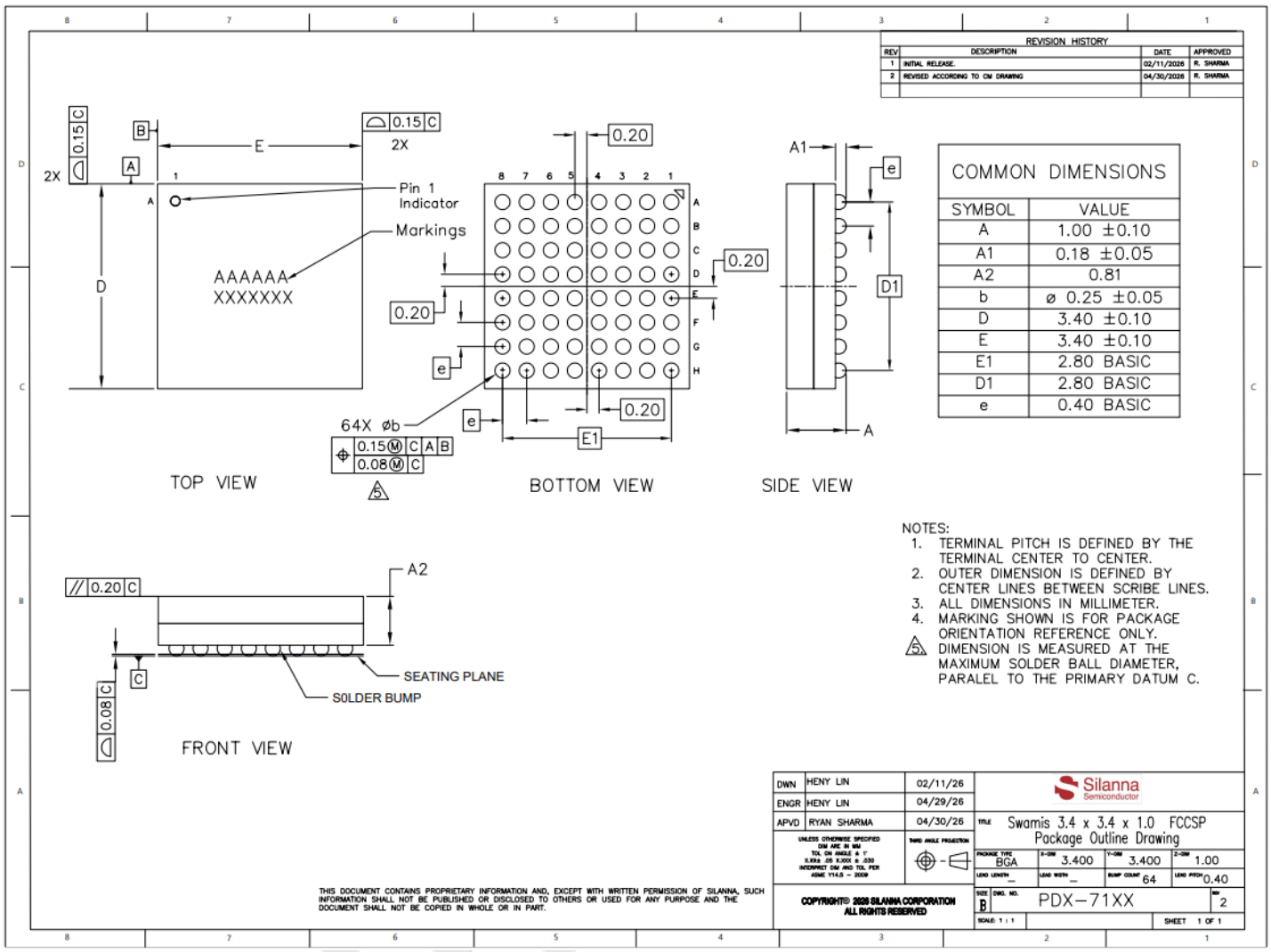


Figure 33: Package Dimensions.

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APPENDIX A: Register Map

This section provides a comprehensive description of the complete register map, detailing all available control and status registers within the device.

0x400 - CHIP_TOP

Address: 0x455		RW	Default: 0x0001
[0]	0x1	Soft reset (active low).	

Address: 0x457		RW	Default: 0x0015
[0]	0x1	Duty Cycle Stabilizer enable (see Duty-Cycle Stabilizer). 0: Disable 1: Enable	
[1]	0x0	Duty Cycle Stabilizer on/off in SPI mode (see Duty-Cycle Stabilizer). 0: Off 1: On	
[2]	0x1	Reserved.	
[3]	0x0	Output disable (see Output Enable). 0: Output enabled 1: Output in high-impedance mode.	
[6:4]	0x1	Reserved.	
[7]	0x0	Software power down. 0: Active State 1: Power Down	
[8]	0x0	Software stand-by mode. 0: Active State 1: Stand-by Mode	

Address: 0x45d		RW	Default: 0x0095
[0]	0x1	ADC reference voltage enable. 0: Disabled 1: Enabled	
[4:1]	0xa	ADC reference voltage value. 0: Lowest ... 15: Highest	
[5]	0x0	Set reference. 0: Internal 1: External from VREF pin	
[11:6]	0x2	Reserved.	
[12]	0x0	Enable selection between Internal and External VREF selection via bit 5. 0: Bit [5] selection disabled 1: Bit [5] selection enabled	
[13]	0x0	Enable selection of VREF out via bit 14. 0: Bit [14] selection disabled 1: Bit [14] selection enabled	
[14]	0x0	Enable VREF pin as reference voltage output. 0: Disabled 1: Enabled	

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Address: 0x463		RW	Default: 0x0019
[0]	0x1	Enable clock receiver. 0: Disable 1: Enable	
[4:1]	0xc	Reserved.	
[7:5]	0x0	Clock RX divider control. 0: Bypass 1: Divide by 2 2: Divide by 3 3: Divide by 4 4: Divide by 5 5: Divide by 6 6: Divide by 7 7: Divide by 8	
[8]	0x0	Enable on-chip 100Ohm termination. 0: Disable 1: Enable	
[9]	0x0	Clock polarity control when DCS is enabled. 0: Disable 1: Invert	
[10]	0x0	Enable SYNC pin synchronization. 0: Disable 1: Enable	

Address: 0x465		RW	Default: 0x0001
[2:0]	0x1	Output data interleaver. 0-5: N/A 6: even-odd interleaving 7: odd-even interleaving	

Address: 0x467		RW	Default: 0x3850
[0]	0x0	LVDS enable. 0: Disable 1: Enable	
[1]	0x0	LVDS reduced swing mode. 0: Disable 1: Enable	
[10:2]	0x14	Reserved.	
[13:11]	0x7	LVDS amplitude. 0: Smallest amplitude 0: ... 7: Largest amplitude	
[15:14]	0x0	Reserved.	

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Address: 0x473		RW	Default: 0x0000
[4:0]	0x0	Reserved.	
[8:5]	0x0	Output data delay in parallel CMOS mode. The output data delay (250ps steps) with respect to the clock	
[9]	0x0	Launching output clock polarity in parallel CMOS mode. 0: Not inverted 1: Inverted	
[13:10]	0x0	Output clock delay. The output clock delay is increased by 250ps * (register value) with respect to the data	
[14]	0x0	Output clock polarity. 0: Not inverted 1: Inverted	

Address: 0x475		RW	Default: 0x0001
[0]	0x1	Enable VCM. 0: Disable 1: Enable	

Address: 0x477		RW	Default: 0x0000
[1:0]	0x0	Sample delay for ADC A data	
[3:2]	0x0	Sample delay for ADC B data	

Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0	Output format. 0: Offset binary 1: Two's complement 2: Gray code 3: Offset binary	
[5:2]	0x0	Output test mode select (see Table 21).	
[6]	0x1	Output test channel. 0: Disable 1: Enable	
[7]	0x1	Reserved.	
[8]	0x0	Output test toggle mode. Toggle between user test pattern 0 and 1.	
[10:9]	0x0	Reserved.	
[11]	0x1	PN9 generator reset (active low).	
[12]	0x1	PN23 generator reset (active low).	
[13]	0x0	Enable the output data scrambler. 0: Disable 1: Enable	
[14]	0x0	Enable alternate bit polarity switch. 0: Disable 1: Enable	

Address: 0x4b7		RW	Default: 0x0092
[15:0]	0x0092	PN9 initial seed.	

Address: 0x4b9		RW	Default: 0x3aff
[15:0]	0x3aff	PN23 initial seed.	

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Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 0.	

Address: 0x4bd		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 1.	

Address: 0x4bf		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 0.	

Address: 0x4c1		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 1.	

Address: 0x4c9		RW	Default: 0x0000
[0]	0x0	Disable auto-recalibration. 0: Disable 1: Enable	
[15:1]	0x0	Reserved.	

Address: 0x4cd		RW	Default: 0x0000
[6:0]	0x0	Reserved.	
[7]	0x0	Enable IQ indicator (Digital IOs). 0: Disable 1: Enable	
[15:8]	0x0	Reserved.	

Address: 0x4cf		RW	Default: 0x0035
[14:0]	0x35	Reserved.	
[15]	0x0	Disable production test mode. 0: Test mode enabled 1: Test mode disabled	

Address: 0x4d3		RW	Default: 0x0007
[3:0]	0x7	LVDS common mode voltage.	
[7:4]	0x0	Reserved.	

Address: 0x4fd	RO	Default: N/A
[2:0]	Chip revision.	
[6:3]	Label ID.	
[8:7]	Reserved.	
[10:9]	Resolution ID for device 0: 10-bit 1: 12-bit 2: 14-bit 3: 16-bit	
[13:11]	Speed ID for device.	

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Address: 0x4ff	RO	Default: N/A
[0]	Reserved.	
[1]	Analog Supply Ready. 0: Not ready 1: Ready	
[2]	Digital Supply Ready.	
[3]	I/O Supply Ready. 0: Not ready 1: Ready	
[4]	Reserved.	
[5]	SPI enabled. 0: Not enabled 1: Enabled	
[6]	Power down pin status. 0: Inactive 1: Active	
[9:7]	Reserved.	
[10]	SYNC pin status.	

0xF00 - ADC_COMMON

Address: 0x809		RW	Default: 0x1800
[11:0]	0x800	A/Q channel gain. 0x000: 0.0 0x800: 1.0 0xfff: 2.0	
[12]	0x1	Enable A/Q path gain and offset.	

Address: 0x80b		RW	Default: 0x1800
[11:0]	0x800	B/I channel gain. 0x000: 0.0 0x800: 1.0 0xfff: 2.0	
[12]	0x1	Enable B/I path gain and offset.	

Address: 0x80d		RW	Default: 0x0000
[15:0]	0x0000	A/Q channel offset. Signed 16-bit two's complement number.	

Address: 0x80f		RW	Default: 0x0000
[15:0]	0x0000	B/I channel offset. Signed 16-bit two's complement number.	

Address: 0xf03		RW	Default: 0x07f9
[0]	0x1	Enable top level bias. 0: Disable 1: Enable	
[3:1]	0x4	Reserved.	
[4]	0x1	ADC enable. 0: Disable 1: Enable	
[10:5]	0x3f	Mask for enable pin.	

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Address: 0xf05		RW	Default: 0x0030
[5:0]	0x30	Mask for stand-by pin.	
[6]	0x0	Reserved.	
[7]	0x0	Stand-by ADC. 0: Disable 1: Enable	

Address: 0xf07		RW	Default: 0x0043
[0]	0x1	Digital clock enable. 0: Disable 1: Enable	
[1]	0x1	Analog clock enable. 0: Disable 1: Enable	
[5:2]	0x0	Reserved.	
[6]	0x1	ADC clock generator reset (active low).	
[7]	0x0	Reserved.	

Address: 0xf09		RW	Default: 0x0040
[2:0]	0x0	Channel B source. 000: ADC B (default) 011: ADC A 111: (ADC A + ADC B)/2	
[5:3]	0x0	Channel A source. 000: ADC A (default) 011: ADC B 111: 0	
[6]	0x1	Reserved.	

Address: 0xf0f		RW	Default: 0x0028
[1:0]	0x0	Clock divider (see Interleave and Decimate Mode. 0: Bypass 1: Divide-by-2 2: N/A 3: N/A	
[5:2]	0xa	Reserved.	

Address: 0xf11		RW	Default: 0x000b
[2:0]	0x3	Reserved.	
[4:3]	0x1	VCM voltage control. 0: Lowest common-mode voltage ... 3: Highest common-mode voltage	

0xDC0 - ADC

Address: 0xdc1		RW	Default: 0xbfff
[3:0]	0xf	Reserved.	
[4]	0x1	Calibration soft reset (active low).	
[15:5]	0x5f9	Reserved.	

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Address: 0xdc3		RW	Default: 0x0000
[3:0]	0x0	Clock phase.	
[14:4]	0x0	Reserved.	

Address: 0xdc9		RW	Default: 0x06a5
[8:0]	0xa5	Reserved.	
[9]	0x1	Stg1 enable background mode.	
[11:10]	0x1	Reserved.	

Address: 0xdcd		RW	Default: 0x1483
[2:0]	0x3	Stg1 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stg1 calibration randomization sequence in foreground mode (see Table 17).	

Address: 0xdcf		RW	Default: 0x0d85
[2:0]	0x5	Stg1 calibration convergence speed in background mode (see Table 17).	
[11:3]	0x1b0	Reserved.	

Address: 0xdd1		RW	Default: 0x02a5
[0]	0x1	Stage 2 gain error calibration enable.	
[1]	0x0	Stage 2 gain error calibration only.	
[8:2]	0x29	Reserved.	
[9]	0x1	Stage 2 enable background mode.	
[11:10]	0x0	Reserved.	

Address: 0xdd3		RW	Default: 0x0bc0
[0]	0x0	Stage 2 force calibration data.	
[3:1]	0x0	Stage 2 calibration data register.	
[6:4]	0x4	Stage 2 bg calibration data register.	
[9:7]	0x7	Stage 2 fg calibration data register.	
[11:10]	0x2	Stage 2 calibration mode.	
[14:12]	0x0	Stage 2 capacitor select register.	
[15]	0x0	Stage 2 cal data magnitude.	

Address: 0xdd5		RW	Default: 0x1483
[2:0]	0x3	Stage 2 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stage 2 calibration randomization sequence in foreground mode (see Table 17).	

Address: 0xdd7		RW	Default: 0x0001
[2:0]	0x1	Stage 2 calibration convergence speed in background mode (see Table 17).	
[11:3]	0x0	Reserved.	

Address: 0xddd		RW	Default: 0x16c3
[2:0]	0x3	Stage 3 calibration convergence speed in foreground mode (see Table 17).	
[11:3]	0xd8	Reserved.	
[13:12]	0x1	Stage 3 calibration randomization sequence in foreground mode (see Table 17).	

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Address: 0xde1		RW	Default: 0xbae8
[7:0]	0xe8	Time allocated for calibration (see Table 17).	
[8]	0x0	Enable calibration (see Table 17).	
[9]	0x1	Enable foreground calibration (see Table 17).	
[10]	0x0	Reserved.	
[11]	0x1	Enable stg1 calibration (see Table 17).	
[12]	0x1	Enable stage 2 calibration (see Table 17).	
[13]	0x1	Enable stage 3 calibration (see Table 17).	
[14]	0x0	Background calibration parallel mode (see Table 17).	
[15]	0x1	Disable background calibration mode for all stages (see Table 17).	

Address: 0xde3		RW	Default: 0x0008
[2:0]	0x0	Reserved.	
[3]	0x1	Clipping control to reserve some headroom for background calibration signals (active low).	

Address: 0xde7		RW	Default: 0x0004
[2:0]	0x4	Reserved.	
[4:3]	0x0	Output data timing. (see Interleave and Decimate Mode)	

Address: 0xdeb		RW	Default: 0x0000
[0]	0x0	Calibration status. 0: Not done 1: Done	
[7:1]	0x0	Reserved.	

Address: 0xdef		RO	Default: N/A
[0]		Calibration complete.	
[15:1]		Reserved.	

0x800 - ADC_DSP

Address: 0x805		RW	Default: 0x0000
[1:0]	0x0	DSP Output clock divider: 00: Disabled (default) 01: Divide by 2 10: Divide by 4 11: N/A	

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Address: 0x807		RW	Default: 0x0300
[0]	0x0	Interleaving Control.	
[6:1]	0x0	Reserved.	
[7]	0x0	Bypass gain correction. 0: Include gain correction 1: Bypass gain correction	
[8]	0x1	Bypass phase correction. 0: Include phase correction 1: Bypass phase correction	
[9]	0x1	Bypass digital down converter (DDC). 0: Include DDC 1: Bypass DDC	
[10]	0x0	Swap I and Q channels. 0: No swap 1: Swap	
[12:11]	0x0	A/Q data delay.	
[14:13]	0x0	B/I data delay.	

Address: 0x811		RW	Default: 0x0000
[9:0]	0x0	IQ phase correction. Signed 10-bit two's complement number. Valid range from -511 to +511.	
[10]	0x0	Enable IQ phase correction. 0: Disable 1: Enable	

Preliminary

Address: 0x813		RW	Default: 0x12a8
[0]	0x0	Enable DDC Q path. 0: Disable 1: Enable	
[1]	0x0	Enable DDC I path. 0: Disable 1: Enable	
[3:2]	0x2	LO1 select: 0: Disabled 1: DDS1 2: DDS2 3: N/A	
[5:4]	0x2	LO2 select: 0: Disabled 1: DDS1 2: DDS2 3: N/A	
[6]	0x0	Low power mode. 0: Disable 1: Enable	
[7]	0x1	LO in low power mode: 0:fs/4 1: fs/2	
[8]	0x2	IQ sum spectral inversion: 0: I*sin 1: I*sin inverted	
[9]	0x0	IQ sum spectral inversion: 0: Q*cos 1: Q*cos inverted	
[10]	0x0	IQ sum spectral inversion: 0: I*cos 1: I*cos inverted	
[11]	0x0	IQ sum spectral inversion: 0: Q*sin 1: Q*sin inverted	
[12]	0x1	IQ sum gain: 0: 1.0 1: 0.75	
[14:13]	0x0	Output data select: 0: bypass 1: I and Q 2: IQ sum 3: LO	

Address: 0x815		RW	Default: 0x0000
[15:0]	0x0000	DDS1 frequency: bits 15:0.	

Address: 0x817		RW	Default: 0x0000
[15:0]	0x0000	DDS1 frequency: bits 31:16.	

Address: 0x819		RW	Default: 0x0000
[15:0]	0x0000	DDS1 frequency: bits 47:32.	

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Address: 0x81b		RW	Default: 0x0000
[15:0]	0x0000	DDS2 frequency: bits 15:0.	

Address: 0x81d		RW	Default: 0x0000
[15:0]	0x0000	DDS2 frequency: bits 31:16.	

Address: 0x81f		RW	Default: 0x0000
[15:0]	0x0000	DDS2 frequency: bits 47:32.	

Address: 0x821		RW	Default: 0x0000
[15:0]	0x0000	DDS1 phase offset. Signed 16-bit two's complement number.	

Address: 0x823		RW	Default: 0x0000
[15:0]	0x0000	DDS2 phase offset. Signed 16-bit two's complement number.	

Address: 0x825		RW	Default: 0x0010
[5:0]	0x10	DDS1 sine amplitude. Signed 6-bit two's complement number.	

Address: 0x827		RW	Default: 0x0000
[5:0]	0x0	DDS1 sine offset. Signed 6-bit two's complement number.	
[11:6]	0x0	DDS1 cosine offset. Signed 6-bit two's complement number.	

Address: 0x829		RW	Default: 0x0000
[5:0]	0x0	DDS2 sine offset. Signed 6-bit two's complement number.	
[11:6]	0x0	DDS2 cosine offset. Signed 6-bit two's complement number.	
[12]	0x0	DDS phase dither enable. 0: Disable 1: Enable	
[13]	0x0	DDS amplitude dither enable. 0: Disable 1: Enable	

Address: 0x82b		RW	Default: 0x0000
[0]	0x0	Load DDS1 frequency. Toggle to load DDS1 frequency.	
[1]	0x0	Load DDS2 frequency. Toggle to load DDS2 frequency.	
[2]	0x0	Load DDS1 phase. Toggle to load DDS1 phase offset.	
[3]	0x0	Load DDS2 phase. Toggle to load DDS2 phase offset.	
[5:4]	0x0	DDS mode: 0: sine 1: saw tooth 2: triangle 3: phase	

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Address: 0x82d		RW	Default: 0x0130
[3:0]	0x0	Reserved.	
[5:4]	0x3	Decimator pulse rate: 0: 1 1: 1/2 2: 1/4 3: N/A	
[8:6]	0x4	Reserved.	

Address: 0x82f		RW	Default: 0x0147
[0]	0x1	Bypass decimator. 0: Do not bypass 1: Bypass	
[1]	0x1	Enable decimator input path A. 0: Disable 1: Enable	
[2]	0x1	Enable decimator input path B. 0: Disable 1: Enable	
[3]	0x0	Enable decimator path C. 0: Disable 1: Enable	
[5:4]	0x0	Decimation factor: 0: 2x 1: 2x, interleaved ADC 2: 4x 3: 4x, interleaved ADC	
[7:6]	0x1	Filter 1 gain: 0: 1.0 1: 0.75 2: 0.5 3: 0.25	
[9:8]	0x1	Filter 2 gain: 0: 1.0 1: 0.75 2: 0.5 3: 0.25	

Preliminary

REVISION HISTORY

Version	Date	Comment
1.0	April 9, 2026	Initial Release.
2.0	November 2, 2026	Updated pin map.

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