

Preliminary Datasheet SL2001

Integrated Resonant Mode Laser Diode Drive System

Features

- Flexible architecture can provide laser FWHM pulses less than 2ns
- Dual Drive Outputs Support Peak Power up to 1000W
- High charging efficiency from a 3V to 24V supply
- Integrates needed blocks for Charging and Firing Resonant Mode Diode Lasers utilizing either EEL Diodes or VCSEL Arrays
- Integrated GAN/MOS Drive for Charging Resonant Capacitor
- Inductor Current Control offers precise Resonant Capacitor Energy even with Input Voltage Fluctuations
- < 5 mW System No Load Power Consumption
- Up to 10 MHz Rep Rate limited by temperature rise in laser and other board components
- Dual Polarity LIGHT Output signal to indicate when laser fires with extremely low jitter (time error jitter < 0.1ns)
- Minimal external components enable extremely integrated and efficient layout
- Integrated I²C interface for Output Power Control and Fault monitoring
- 7 MTP Bytes (3 time programmable) for fault and timing settings
- 218 OTP Bytes for customer usage
- 1 mm x 3.5 mm WLCSP Package

Applications

- Laser TOF Measurement Systems
- LIDAR Array
- Range Finding

- 3D Mapping
- ADAS

Product Description

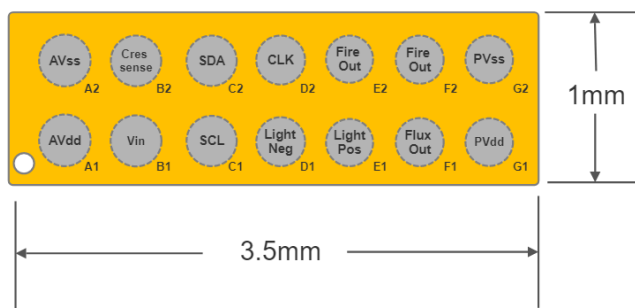
The SL2001 is an Integrated Boost Supply, Timing Controller and Driver for Laser Time-of-Flight Measurement Systems employing Edge Emitting Laser Diodes or VCSEL Arrays.

This device provides the ease-of-design of a simple resonant flash TOF laser system but is integrated together with a boost charger and proprietary charge control to efficiently charge the resonant capacitor to the optimum voltage and a GANFET Driver to fire the laser.

The integrated Pulse Timing Controller uses a proprietary Architecture to provide Laser Diode pulses less than 3 ns wide with over 400 watts of output power. An External MOSFET or small GANFET provides the “Flash” signal to fire the laser, an output trigger signal provides an accurate start trigger for Time-of-Flight measurements. Dual Fire OUT pins are Provided for Higher Power Applications with multiple Laser Diodes

The Resonant Capacitor is charged during each pulse cycle via an internal boost charger. This integrated charging architecture minimizes losses normally associated with transferring charge from standard High Voltage Supply Rails. The supply voltage for the charger can be as low as 3 volts and still achieve laser diode anode voltages of > 80 volts.

I²C adjustment for setting the amount of charge in the resonant capacitor to regulate light power. Fuse option to also adjust output power via charger input voltage. Output power can be tightly regulated by the charging circuit. With this high level of integration, it is possible to achieve the highest light power with optimum efficiency.



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Pin Out

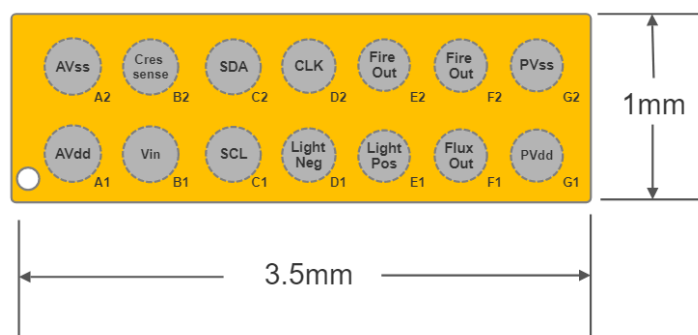


Figure 1: SL2001, 14 ball WCSP (0.5mm ball pitch) – Device Top View (bumps down)

Pin Definitions

Pin #	Name	Voltage Category (Vdc)	Description
A1	AVdd	LV: (5V)	Analog supply for inputs
A2	AVss	LV (0)	analog ground for inputs
B1	VIN	MV (24V)	inductor input voltage sense point
B2	Cres_SNS	LV (5V)	Cres voltage sense via external impedance
C1	SCL	LV (5V)	I ² C clock pin
C2	SDA	Output LV	I ² C data pin
D1	LIGHT NEG	Output LV	Output indicating Laser Firing. low on rising edge of FireOUT and stays low for 75ns or until FireOUT goes low
D2	CLK	LV (5V)	Dual function timing input for capacitor charge and laser firing (see Figure #)
E1	LIGHT POS	Output LV	Output indicating Laser Firing. high on rising edge of FireOUT and stays high for 75ns or until FireOUT goes low
E2	FireOUT	Output LV	Output Drive for MOSFET or EGAN FET for External Cathode Clamp
F1	FluxOUT	Output LV	Output Drive for MOSFET or EGAN FET for External Cathode Clamp
F2	FireOUT	Output LV	2 nd FireOUT pin (shorted to pin E2) for lower board impedance to FET gate
G1	PVdd	LV: (5V)	Power Supply for gate drive outputs
G2	PVss	LV (0)	Power Resonant Supply Voltage Rail Return for gate drive outputs

Functional Block Diagram

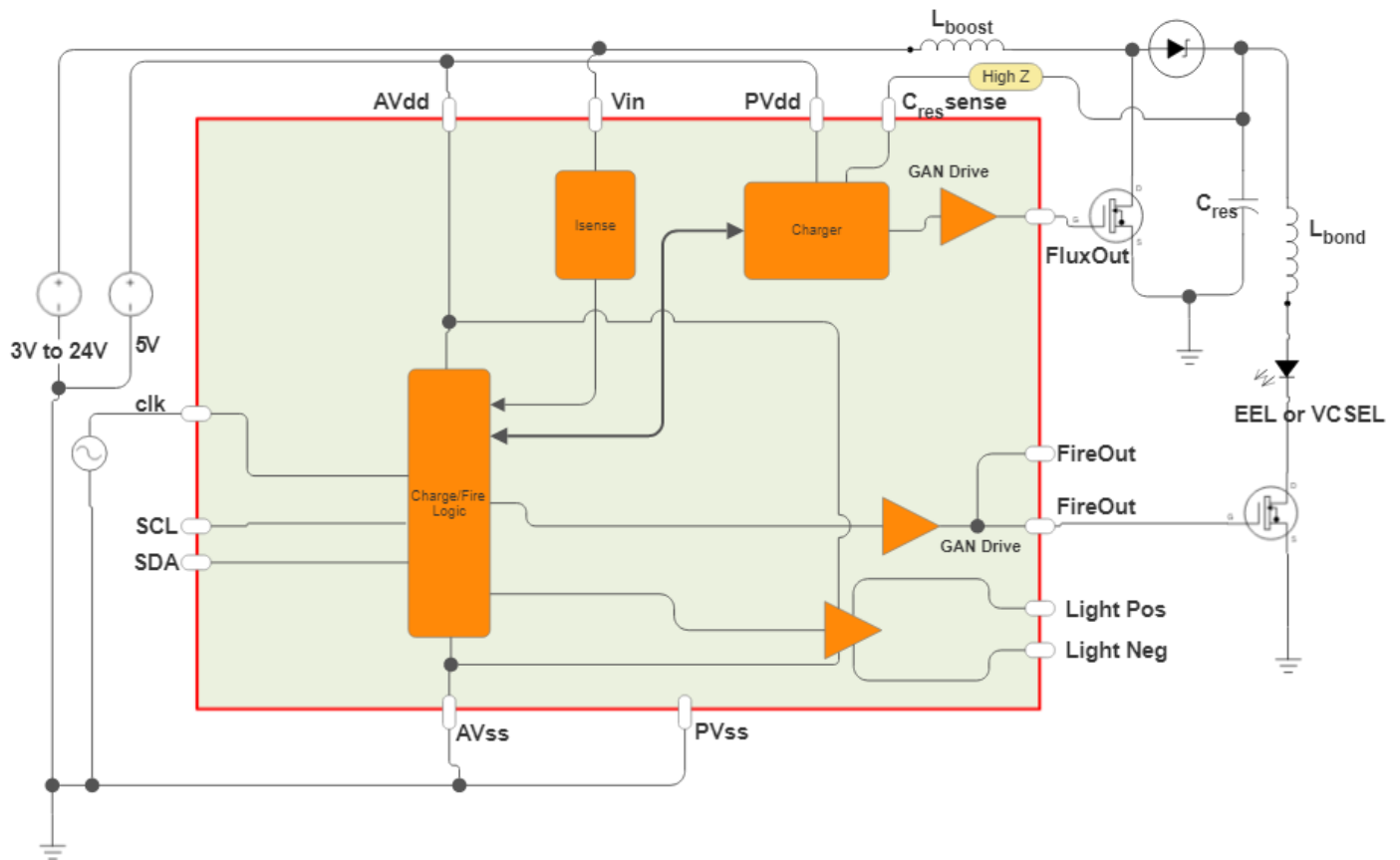


Figure 2: Functional Block Diagram

Figure 3: Typical Application Circuit

Absolute Maximum Ratings ^{Note 1}

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Max.	Units
Pin Voltages - Inputs	CLK		-0.3	AVdd+0.3	V
	AVdd		-0.3	6.5	
	AVss		-0.3	0.3	
	PVdd		-0.3	6.5	
	PVss		-0.3	0.3	
	SCL, SDA		-0.3	AVdd+0.3	
	Cres_SNS		-0.3	AVdd+0.3	
	VIN		-0.3	28	
Pin Voltages - Outputs	FireOUT		-0.3	6.5	V
	LightPOS,LightNEG		-0.3	6.5	
	FluxOut		-0.3	6.5	
Storage Temperature	T _{STG}		-50	150	°C
Junction Temperature	T _J		-40	150	
Lead Temperature ⁽³⁾	T _{LEAD}			260	
Electrostatic Discharge (ESD) Protection ⁽⁴⁾⁽⁵⁾	V _{ESD}	HBM, Human Body Model per ANSI/ESDA/JEDEC JS-001	-2000 ⁽⁶⁾	2000 ⁽⁶⁾	V
		Charged-device model (CDM), per JEDEC specification	-500	500	V

Notes:

- 1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- 2) 1/16" from the case.
- 3) JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- 4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information Note 1

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	30	°C/W
Thermal Resistance Junction to Board	$R_{\theta JB}$	12	

Notes:

- 1) Simulated on 2S2P JEDEC 51-7 board.

Recommended Operating Conditions Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Vdd Supply Input Voltage	V_{Vdd}		4.5	5	6.0	V
VIN Voltage	V_{IN}		2.7		24	V
AVdd Bypass Capacitor	C_{AVdd}		0.1	-	10	μF
PVdd Bypass Capacitor	C_{PVdd}		0.1	-	10	μF
Vin Bypass Capacitor	C_{Vin}		10	-	-	μF
Operating Junction Temperature	T_J		-40		125	°C

Notes:

- 1) Device electrical characteristics are not guaranteed outside the recommended operating conditions.
- 2) Note that many electrical characteristics are specified for $4.5V < V_{dd} < 5.5V$

Electrical Characteristics

(Unless otherwise specified, $4.5V < AVDD < 5.5V$, $AVDD = PVDD$, $T_J = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ recommended operating conditions.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Current (Vdd)						
Input Supply Current, No Load	$I_{VDD(NL)}$	Laser fire freq < 1kHz, DAC codes 150	-	1.0	-	mA
Input Supply Current, Pulsing	$I_{VDD(SW)}$	Laser fire freq = 250kHz?, Fire Out cap = 100pF ¹	-	3	-	mA
FireOut Drive Output – the two FireOut bumps are shorted on die						
FireOut Resistance Pull Down	$R_{DSL_FireOut}$	$I_{OL_FireOut} = 100\text{mA}$			180	mΩ
FireOut Resistance Pull Up	$R_{DSH_FireOut}$	$I_{OH_FireOut} = 100\text{mA}$			250	mΩ
Peak Sink Current	$I_{OL_FireOut}$	$V_{OL_FireOut} = 5V$ ¹		12	-	A
Peak Source Current	$I_{OH_FireOut}$	$V_{OH_FireOut} = 0V$ ¹		10		A
FluxOut Output						
FluxOut Resistance Pull Down	$R_{DSL_FluxOut}$	$I_{OL_FluxOut} = 100\text{mA}$			720	mΩ
FluxOut Resistance Pull Up	$R_{DSH_FluxOut}$	$I_{OH_FluxOut} = 100\text{mA}$			1	Ω
Peak Sink Current	$I_{OL_FluxOut}$	$V_{OL_FluxOut} = 5V$ ¹		3	-	A
Peak Source Current	$I_{OH_FluxOut}$	$V_{OH_FluxOut} = 0V$ ¹		2.5		A
LIGHT Drive Output – same parameters for LightPOS & LightNEG pins						
LIGHT Resistance Pull Down	R_{DSL_LIGHT}	$I_{OL_LIGHT} = 100\text{mA}$			1.44	Ω
LIGHT Resistance Pull Up	R_{DSH_LIGHT}	$I_{OH_LIGHT} = 100\text{mA}$			2	Ω
Peak Sink Current	I_{OL_LIGHT}	$V_{OL_LIGHT} = 5V$ ¹		1.5	-	A
Peak Source Current	I_{OH_LIGHT}	$V_{OH_LIGHT} = 0V$ ¹		1.25		A
FireOut Switching Parameters						
Maximum Switching Frequency ⁽¹⁾	f_{SW_MAX}	Note 1			10	MHz
Minimum On Time	T_{ON_MAX}	Minimum on time of the FireOut FET gate driver ¹	1			ns
LightPos & LightNeg output parameters						
Delay from FireOut rise to LightPos rise or LightNeg Fall		crossing threshold through 50% of Vdd ¹	-1		1	ns
FireOut to LIGHT rise cycle to cycle jitter		crossing threshold through 50% of Vdd with 100pF load on FireOUT & 10pF load on LightPos/Neg ^{1,2}	-100		100	ps
LightPos high & LightNeg low pulse width		crossing threshold (AVdd – Avss) / 2	35		105	ns
Input Signal Parameters						
CresSNS resistance to AVss		While operating; forced to 0.2V		22		kΩ
CLK input rising threshold			1.7		2.6	V
CLK input falling threshold			1.1		1.8	V
CLK input voltage hysteresis			0.5		1	V
SDA/SCL input rising threshold					1.7	V
SDA/SCL input falling threshold			0.45			V
I ² C SCL Frequency					1	MHz
Timing Parameters						
CLK high to FluxOUT		CLK >50% to FluxOUT > 50%		5		ns
FluxOUT PW range from FluxOUT>50% to FluxOUT<50%		typ values for range, see Basic Timing Description Section explanation ¹	5		2800	ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FluxOUT PW Accuracy from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, VIN=5V	188	200	212	ns
FluxOUT PW jitter from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, VIN=5V ^{1,2}	-1		+1	%
CLK high to FluxOUT jitter from Clock>50% to FluxOUT>50%		DAC code h'A8 on Flux Time Reg cycle to cycle jitter; 100pF on FluxOUT ^{1,2}	-2.5		+2.5	ns
FluxOUT rise time		20% to 80% of PVdd 100pF on FluxOUT ^{1,2}		0.45		ns
FluxOUT fall time		80% to 20% of PVdd 100pF on FluxOUT ^{1,2}		0.45		ns
FluxOut Low to FireOut High range from FluxOUT<50% to FireOUT>50%		typ values for range, see Basic Timing Description Section explanation ¹	10		2800	ns
FluxOut Low to FireOut High Accuracy from FluxOUT<50% to FireOUT>50%		DAC code h'A7 on Charge Time Reg 100pF on FluxOUT & FireOUT ³		200		ns
CLK low to FireOut		CLK <50% to FireOUT > 50% ¹		20		ns
FireOut PW range from FireOUT>50% to FireOUT<50%		typ values for range, see Basic Timing Description Section explanation ¹	1		320	ns
FireOut PW Accuracy from FireOUT>50% to FireOUT<50%		DAC code h'80 on Fire Time Reg, 100pF on FireOUT, VDD=5V, T=25C ¹	4.25	5	5.75	ns
FireOut PW jitter from FireOUT>50% to FireOUT<50%		DAC code h'7C on Fire Time Reg 100pF on FireOUT ^{1,2}	-4		+4	%
CLK low to FireOut jitter from Clk<50% to FireOUT>50%		DAC code h'7C on Fire Time Reg cycle to cycle jitter; 100pF on FireOUT ^{1,2}	-5		+5	ns
Supply Voltage Threshold and Fault Protection Parameters						
AVdd & PVdd rising threshold		Vth bits set to 00	4.2	4.35	4.5	V
		Vth bits set to 01	2.5	2.6	2.7	V
		Vth bits set to 10	2.8	2.9	3	V
		Vth bits set to 11	4.6	4.8	5	V
AVdd & PVdd falling threshold		Vth bits set to 00	3.9	4.05	4.2	V
		Vth bits set to 01	2.2	2.3	2.4	V
		Vth bits set to 10	2.5	2.6	2.7	V
		Vth bits set to 11	4.3	4.5	4.7	V
AVdd & PVdd Vth Hysteresis				0.24		V
delay from Vdd rising threshold to laser firing enabled		Note 1			1	ms
Vin Over Voltage accuracy		threshold setting programmable per Table 7	- 7.5		7.5	%
Vin Under Voltage accuracy		threshold setting programmable per Table 6	- 7.5		7.5	%
Thermal Shutdown (OTP)	T _{SD}	Note 1	125			°C
Thermal Shutdown Hysteresis	T _{HYS}	Note 1		20		°C
Cres pre-Charge OV		threshold setting programmable per Table 48	-tbd		+tbd	%
Cres post Charge OV		threshold setting programmable per Table 48	-tbd		+tbd	%
Cres pre-charge UV		threshold setting programmable per Table 48 Vin = 5V, Rsns=6.8MΩ, Vth setting value 2	-tbd		+tbd	V
Cres post-charge UV		threshold setting programmable per Table 48	-tbd		+tbd	%

Parameter	Symbol	Condition	Min	Typ	Max	Unit

Notes:

- 1) Guaranteed by design and characterization, not production tested
- 2) cycle to cycle jitter is specified for no change in any environmental conditions. It shows a Gaussian distribution with 3 sigma numbers specified as limits
- 3) Only valid for operating mode where CLK falling edge does NOT trigger the laser to fire.

Detailed Descriptions

Overview

The SL2001 is a fully integrated Resonant Mode Controller for Driving EEL or VCSEL Laser Diodes. The SL2001 provides a predetermined amount of charge to the laser resonant capacitor each cycle from a low input voltage source allowing the resonant capacitor voltage to increase as a function of the amount of charge. It is possible to achieve high resonant capacitor voltage from a relatively low input V_{in} . Resonant Capacitor values which match the small predicted parasitic inductance values can be used. This eliminates the need for a boost converter to provide the needed high Resonant Capacitor Voltage. A series inductor is used to provide the current to charge the Resonant Capacitor to the needed voltage for the Laser Diode resonant circuit. The stored energy in the Resonant Capacitor is then transferred to the Laser Diode during the "Firing" phase. The SL2001 monitors the input Voltage (V_{in}) and adjusts the amount of time the input inductor is "fluxing" to compensate for variations in V_{in} . Fault trigger levels can be set for V_{in} undervoltage and overvoltage. The SL2001 also monitors the voltage on the Resonant Capacitor (Cres) for under and over voltage conditions. These Fault trigger points are set via internal registers and programmed over the I²C interface. A description of the Fault detection and operation is shown in [Figure 18: SL2001 Fault Diagram](#).

Detailed Pin Descriptions

Pins A1: AV_{dd} and A2: AV_{ss}

AV_{ss} is the Main ground return for the analog circuitry and the LIGHT_OUT signals. This circuitry is supplied by AV_{dd} , a decoupling capacitor between AV_{dd} and AV_{ss} should be placed as close as possible to the IC. AV_{ss} should nominally be tied to board ground within a few millimeters of the SL2001 in a board location that is outside of the current path between the ground input to the board and the ground of the resonant capacitors. Special attention should be paid to preventing switching noise between AV_{ss} and the ground pins of the chip that is receiving the LIGHT_POS and LIGHT_NEG output signals.

Pins G1: PV_{dd} and G2: PV_{ss}

PV_{ss} is the main power ground return for the gate drive circuitry. The gate drive circuitry is supplied by PV_{dd} . A decoupling capacitor between PV_{dd} and PV_{ss} should be placed as close as possible to the IC. PV_{ss} should be tied to the power ground plane in a manner to minimize inductive voltage ringing between the GaN FET used for laser firing (1st priority) as well as minimize the inductive voltage ringing between the GaN FET used for inductor current ramp (2nd priority).

Pin B1: V_{in}

This pin is used to sense the inductor input voltage for Fault recognition as well as to maintain a constant inductor peak current. The V_{in} over voltage and under voltage Fault Thresholds are set via register 0X13.

Pin B2: Cres_SNS

The Cres_SNS pin is used to sense the high voltage across the resonant capacitor utilizing an external resistor as shown in [Figure 19](#). Value options include 6.2M Ω or 6.8M Ω , with the fault threshold voltages varying per [Table 8](#). Please ensure that the external resistor can support the maximum voltage on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2001 takes when a fault is detected is described in [Table 4: Fault Conditions](#)

Pins C1: SCL and C2: SDA

These are Clock and Data pins for I²C interface. The I²C Interface is always accessible. Please see [Table 3](#) **Error! Reference source not found.** Four selectable I²C addresses are available for the SL2001. These are selected by changing bits 1 & 0 in register address 0x16. These bits can be changed via an I²C command, in which case the address will change immediately such that all subsequent I²C communication will use the new address. The address bits can also be loaded into the 3-time programmable MTP such that the I²C address option will always be loaded at part start-up, explained in [Table 1](#).

Register 0x16 bit1 bit0	I ² C Address
00	0001001x
01	0101001x
10	1001001x
11	1101001x

Table 1: I²C Startup Addresses

Pins D1: LIGHTNEG and E1: LIGHTPOS

These pins provide an indication of the **FireOUT** signal going high with an extremely small amount of signal jitter from period to period (3 sigma jitter <100ps).

Pin D2: CLK

This multi-function pin supplies the main clock to the pulse timing generator. The rising and falling edges of the clock can be programmed to trigger the gate drive outputs in 3 different modes as described in the timing control section below in [Figure 4: Mode1 Timing](#).

Pins E2 and F2: FireOUT

These pins provide an extremely fast gate drive signal with adjustable pulse width between 0.5ns and 100ns for the GaN or MOS Gate Drive. Two adjacent pins are used to reduce the parasitic inductance on the die and on the board.

Pin F1: FluxOUT

This pin provides a fast gate drive signal with adjustable pulse width between 5ns and 1μs for the GaN FET that is used to ramp current in the inductor and charge the resonant capacitor.

Timing Description for Flux, Charge and Fire

Mode1 Timing Steps

The **CLK** rising edge triggers **FluxOUT** to rise, starting the Flux time (inductor current ramp). The Flux time “Tflux(ns)” is controlled by register 0x10 with 2.5% steps from 5ns to 2.8μs as shown in [Figure 8: Flux Time vs. DAC Code](#). At the falling edge of the **FluxOUT** signal (end of Flux time), the Charge time begins. The Charge time “Tcharge(ns)” is controlled by register 0x11 with 2.5% steps from 10ns to 2.8μs as shown in [Figure 14](#). At the end of the Charge time, the FireOUT signal goes high to begin the Fire time. The Fire time “Tfire(ns)” is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in [Figure 4](#).

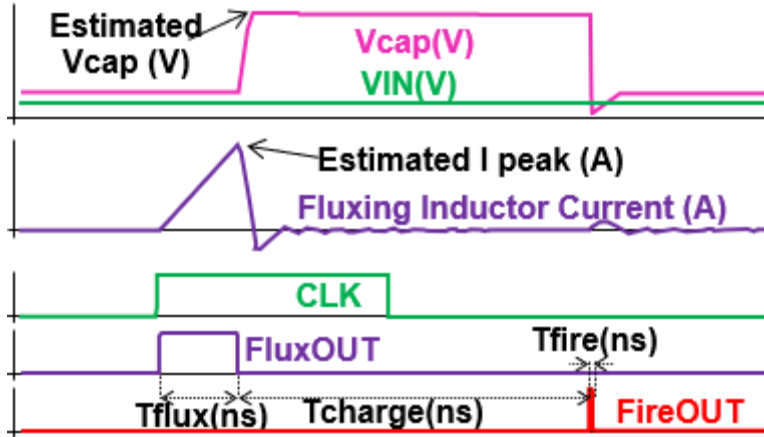


Figure 4: Mode1 Timing

Mode2 Timing Steps

CLK rising edge triggers **FluxOUT** to rise, starting the Flux time (inductor current ramp). The Flux time “Tflux(ns)” is controlled by register 0x10 with 2.5% steps from 5ns to 2.8μs as shown *Figure 8*. The Charge time “Tcharge(ns)” is controlled by the pulse width of the **CLK** input pin. At the falling edge of the **CLK** input pin, the **FireOUT** signal goes high to begin the Fire time. The Fire time “Tfire(ns)” is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in *Figure 8: Flux Time vs. DAC Code*.

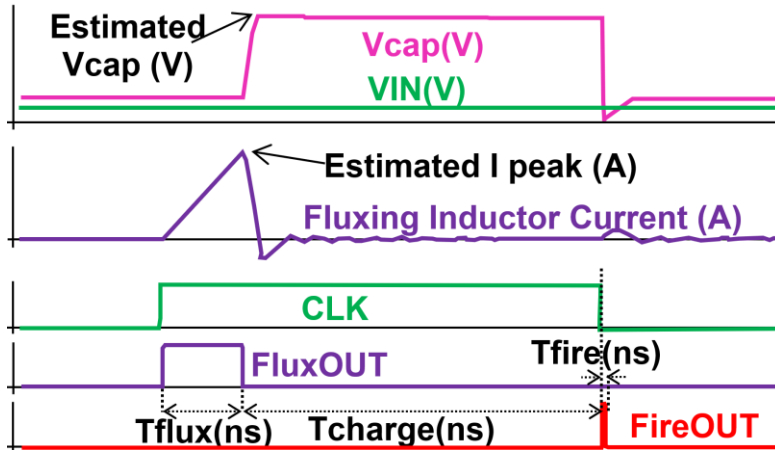


Figure 5: Mode2 Timing

The timing for Fluxing, Charging (mode1 only), and Firing is controlled by the circuit in *Figure 6*. A current (I1) is set-up by forcing a voltage (Vref1) across a DAC programmable resistance value. That current (I1) is then mirrored to a current I2 and used to charge a capacitance to a voltage level (Vref2). When the **CLK** signal goes high, the **Fluxout** signal will go high until the capacitor is charged to the Vref2 level. The **Fluxout** high time will follow the equation:

$$\text{Equation 1 : Fluxout high} = \frac{C * Vref2 * Rdac}{Vref1 * Gmirror}$$

The **Fluxout** high time will change proportionally to a change in the DAC resistance value (Rdac). The **Fluxout** high time will change inversely proportional to a change in the voltage of Vref1 or the gain of the current mirror (Gmirror).

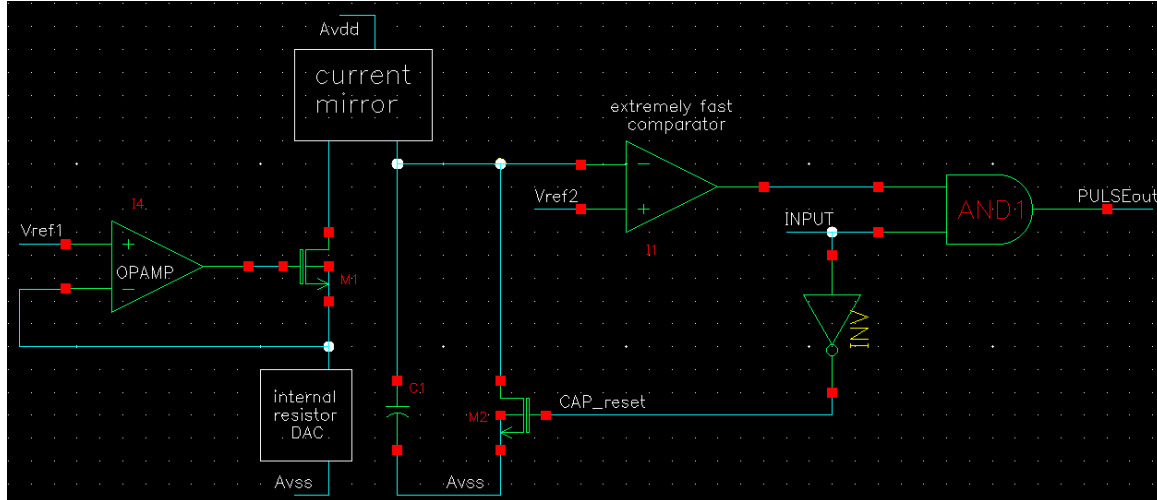


Figure 6: Flux Timing Generation

Three 8-bit registers (0x10h, 0x11h, 0x12h): FluxTime, ChargeTime and FireTime correspond to DACs for each of these timing parameters. Their resistor value increases by ~2.5% for each DAC step, with a minimum resistor value of 2kΩ and a maximum resistor value of 1.085MΩ with each resistor value set by Equation 2 for Rdac codes from zero to 255.

$$\text{Equation 2: } R_{dac} \text{ value} = 2k * 1.025^{(R_{dac} \text{ code})}$$

the Rdac value changes linearly on a log scale as shown in the graph in Figure 7. Note that the Rdac code is an exponent in the equation above.

DAC resistance setting vs DAC code (log scale)

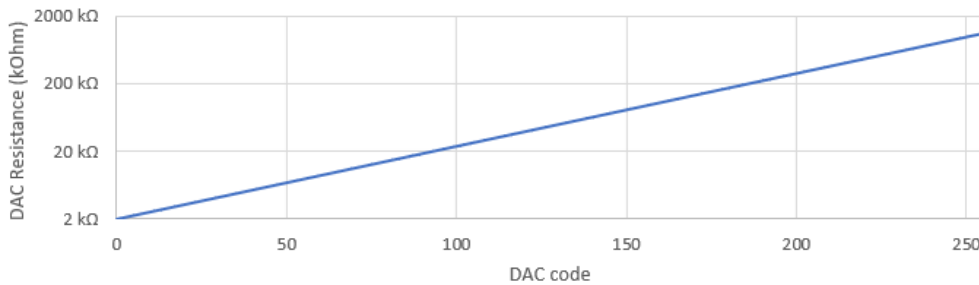


Figure 7: DAC Resistance Setting vs. Code

The equation for peak inductor current (I_{L_peak}) verses Flux time (T_{flux}) is:

$$\text{Equation 3: } I_{L_peak} = V_{in} * \frac{T_{flux}}{L}$$

The Flux time setting can be set to vary inversely with the V_{in} voltage or to be fixed and not change as V_{in} changes. The Flux time varies inversely with the V_{in} voltage shown in Figure 8: Flux Time vs. DAC Code. This maintains a constant peak inductor current (I_{L_peak}).

The V_{in} dependent Flux time can be set for an average V_{in} voltage of either 5V or 12V. For the 5V setting, the Flux time will automatically change inversely to V_{in} over a V_{in} range of 3.5V to 7.5V. For the 12V setting, the Flux time will automatically change inversely to V_{in} over a V_{in} range of 8.4V to 18V. If V_{in} strays beyond the range settings above (for example, >7.5V for V_{in} dependent 5V setting), there is a risk that Flux time will no longer change to correct for changes in V_{in} allowing the inductor current peak to also change proportional to V_{in} .

The graph below in *Figure 8: Flux Time vs. DAC Code* shows the behavior of the Flux Time to the V_{in} voltage. The orange curve has longer Flux time due to the lower V_{in} voltages (3.5V for the 5V setting and 8.4V for the 12V setting), while the red curve has a shorter Flux time due to the higher V_{in} voltages (7.5V for the 5V setting and 18V for the 12V setting).

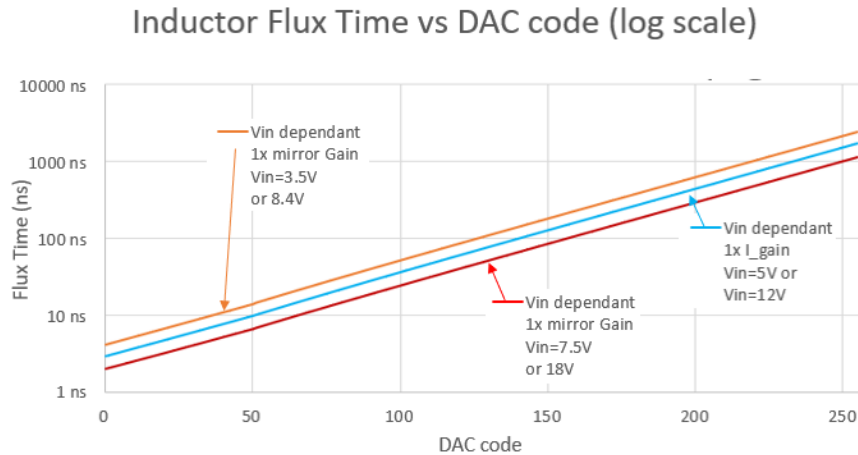


Figure 8: Flux Time vs. DAC Code

Because the Flux time varies inversely with the V_{in} voltage, the peak inductor current (I_{L_peak}) will be constant for a given value of inductance per *Equation 3*. Tflux is the same for the 5V & 12V settings, the I_{L_peak} will be higher with 12V than for 5V according to

$$\text{Equation 3: } I_{L_peak} = V_{in} * \frac{T_{flux}}{L}$$

The graph in *Figure 9: Peak Current vs. DAC Code* below shows the Tflux with Gmirror=1 & 440nH inductor or Gmirror=2 & 220nH inductor.

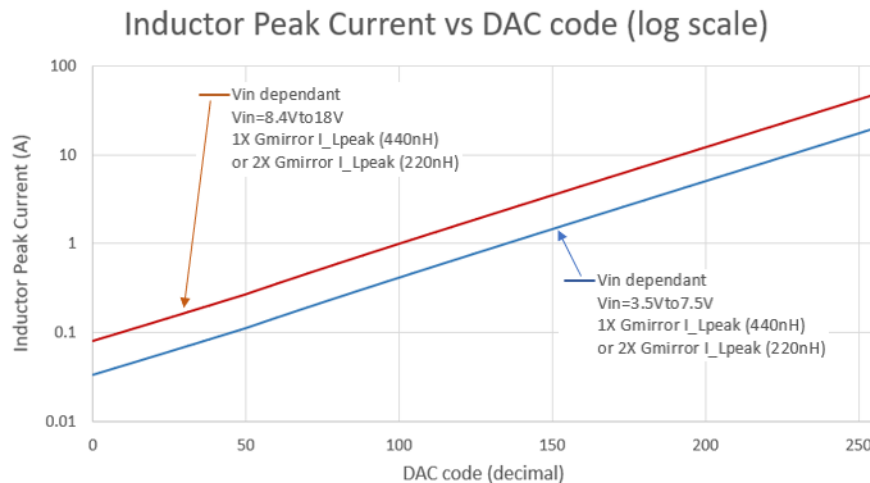


Figure 9: Peak Current vs. DAC Code

For smaller values of inductors, a 2x Gmirror setting is available. This mode almost doubles the current into the capacitor of *Figure 10*, which decreases Flux Time for a given DAC setting by a factor of ~1.8. Users can use the I²C interface to adaptively change the DAC resistor setting which varies the Inductor Flux time (Tflux). This will change the inductor peak current (I_{L_peak}) which in turn will increase or decrease the voltage of the resonant capacitor (C_{res}) and the current through the laser diode when it is fired. For customers who want to adaptively change the peak inductor current (I_{L_peak}), but do not want to use the I²C interface, an option is included where the part does not automatically vary the Flux time (Tflux) as V_{in} varies. With this option, the customer can vary V_{in} to change the inductor peak current (I_{L_peak}) according to *Equation 3*.

The graph in [Figure 10: Flux Time Independent upon](#) below shows the inductor flux time (T_{flux}) for the mode where the Flux time is independent of V_{in} for the 1x and 2x current mirror gain (G_{mirror}) settings.

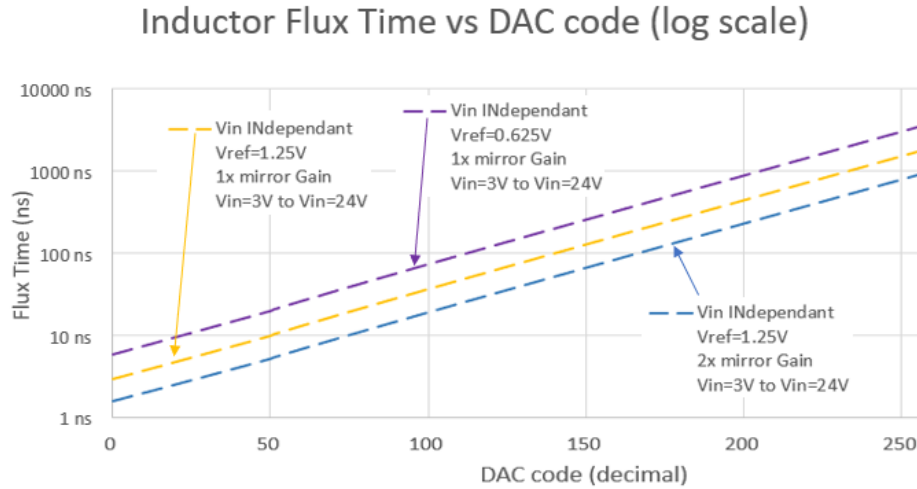


Figure 10: Flux Time Independent upon V_{in}

Since the Flux time is not changing as the V_{in} voltage changes, the peak inductor current (I_{L_peak}) will change for a given value of inductance per [Equation 5](#). The Graph in [Figure 10: Flux Time Independent upon](#) above shows the Flux Times at different values of V_{in} with a $G_{mirror}=1$ and a 440nH inductor or $G_{mirror}=2$ and a 220nH inductor.

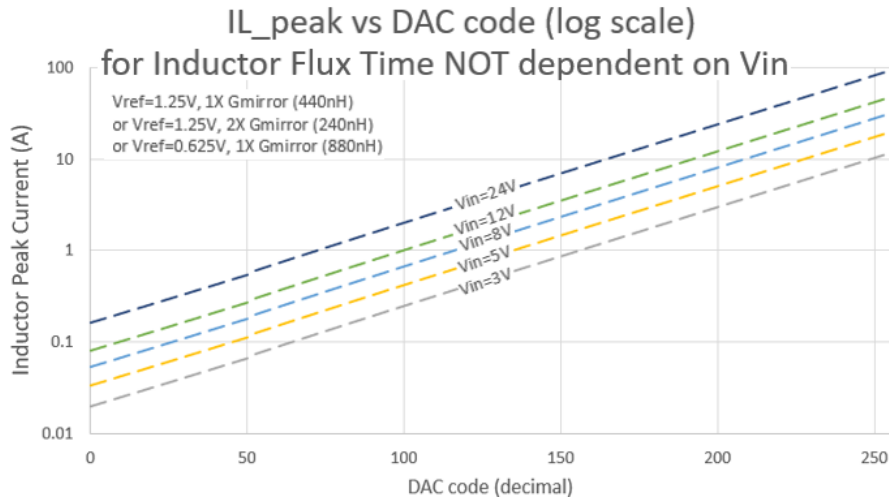


Figure 11: Flux Time Independent upon V_{in}

Shown in [Figure 12](#), the Schottky Anode Voltage is pulled to Ground during the Fluxing time such that the voltage across the inductor is fixed to $V_{in} - 0V = V_{in}$. Using [Equation 4](#) and knowing that the inductor current at the beginning of the Fluxing time is always zero, we can define the equation components as $V = V_{in}$, L =inductor value dt =Fluxing time. By rearranging the equation, we can solve for the inductor current at the end of the Fluxing period, [Equation 5](#).

$$\text{Equation 4: } i_L = \frac{V}{L} \int_0^{T_{flux}} dt$$

$$\text{Equation 5: } I_{Lpeak} = V_{in} * \frac{T_{flux}}{L}$$

The default setting for the fluxing time control of the SL2001 uses the equation above to maintain a constant peak inductor current at the end of the Fluxing time (I_{L_peak}) by changing the Fluxing time inversely proportional to changes in the V_{in} voltage.

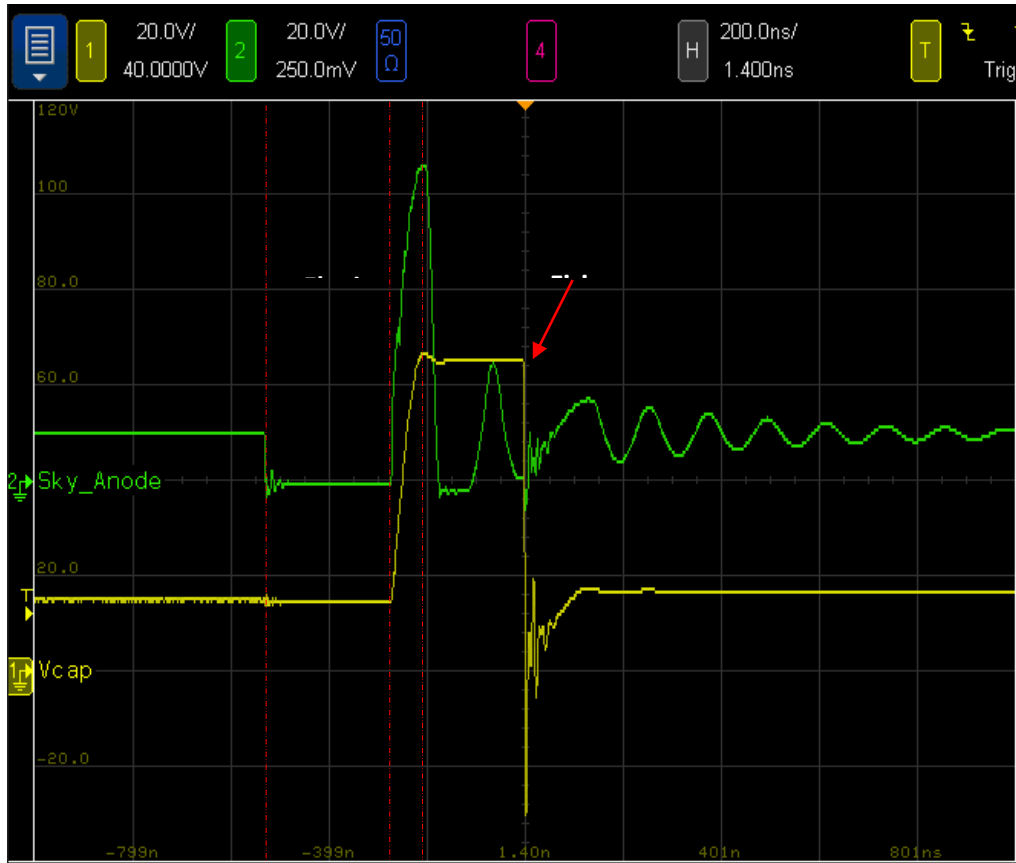


Figure 12: Firing Sequence

During the Charging time, the inductor current returns to zero as the resonant capacitor voltage is rising to a voltage above V_{in} . The charge applied to the resonant capacitor during this time is equal to $Q=I \cdot \text{time}$, so a constant capacitor charge level can be maintained by changing current and charging time inversely proportional to each other. Since the peak current drops proportionally to changes in the inductor value, the Fluxing time will need to change by the square root of any change to the inductor value. For example, if the inductor value is doubled (2x) and the Fluxing time is increased by the square root of 2, then the inductor current at the end of the Fluxing time will change per the following equation:

$$\text{Equation 6: } I_{Lpeak} = T_{flux} * \frac{\sqrt{2}}{2 * L}$$

but the charging time Δt will increase per the following equation

$$\text{Equation 7: } \Delta t = \frac{I_{Lpeak}}{\sqrt{2}} * 2L$$

going back to the charge equation $Q = I * \text{time}$, we see that the charge will change by

$$\text{Equation 8: } \frac{I_{Lpeak}}{\sqrt{2}} * \text{time} * \sqrt{2} = 1$$

so the charge supplied to the capacitor has not changed.

Since the Fluxing time needs to increase by the square root of any increase in the inductor value to maintain a constant charge to the resonant capacitor, the user can input an inductor value range that the SL2001 will use to set the on-time. The inductor range settings do not need to match with the exact inductor value and they are simply used to modify the available range and step sizes for Fluxing time. The optional inductor range values are shown in [Table 2](#).

For proper operation of the adjustment for on-time versus V_{in} , the range is limited to around 5V (3.4V to 6.8V) or 12V (8V to 16V). The user can use the I²C and MTP address bits below to achieve 3 different fixed Flux time ranges.

decimal code	00x15 bit3=1 00x15 bit0=0	00x15 bit3=0 00x15 bit0=0	00x15 bit3=0 00x15 bit0=1
fixed Flux time range	low range	middle range	high range

Table 2: Flux Inductor Ranges

Based upon the Flux time range settings above, the user can program the peak current at the end of the Fluxing time per Table 2.

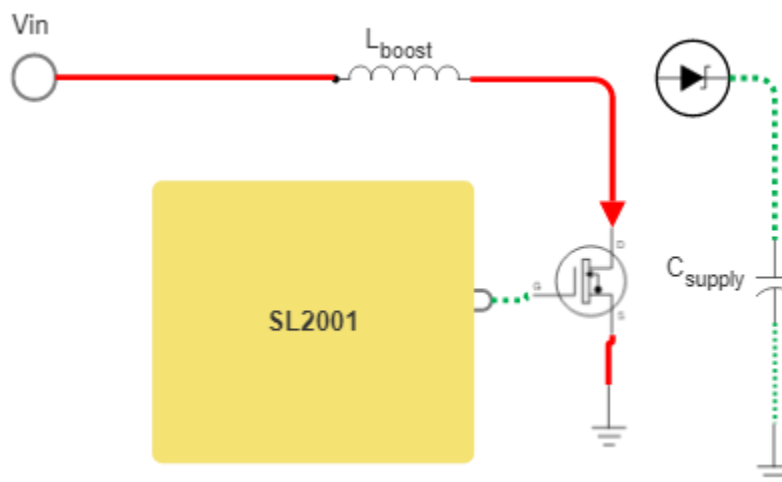


Figure 13: Fluxing Phase

For mode 1 described above, the Charge Time (the time between the Cres voltage rising and the laser firing) is set with the same formula as the Flux time; however, each charge time will be ~4ns longer than the same code setting for Flux Time. Due to internal noise, the Charge time may vary during operation to as much as 25% below the set time range. This does not affect the peak light current from the laser. Figure 14 below shows the Charge Time versus DAC code for mode 1.

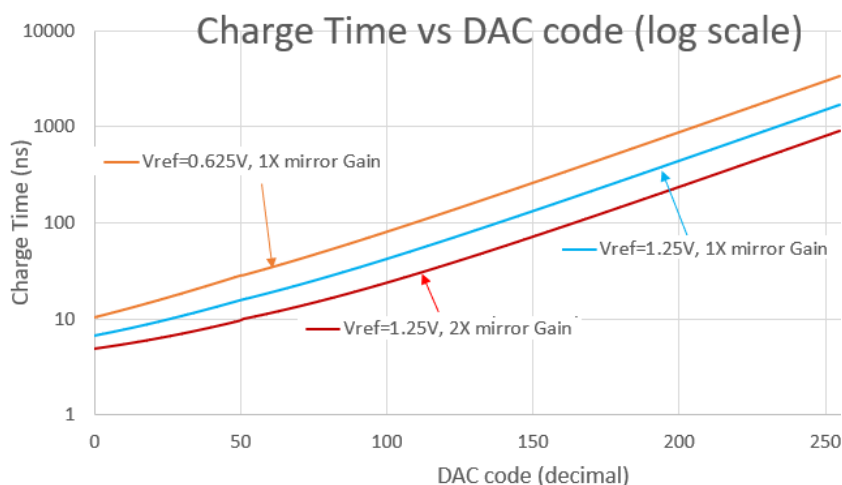


Figure 14: Charge Time set by Clock Duty Cycle

For mode 2 described above, the Charge Time is set via the duty cycle of the clock.

The Charge Time should be set high enough to cover the post charge blanking times for the Cres sense overvoltage and undervoltage circuitry, which is ~400ns. 1 μ s is a good typical setting since it is not long enough to get any noticeable voltage degradation in Cres after charging while also covering the Cres sense blanking times with sufficient margin.

The Pulse Width of the **FireOUT** signal can be adjusted to balance between keeping the gate ON long enough to reach peak laser current and not violate the negative voltage requirements of the laser while at the same time turning OFF quickly enough to prevent a 2nd pulse of light through the laser. *Figure 15: Fire Time Set by Clock Duty Cycle* Figure 15 below shows the Fire Time versus DAC code for the 3 possible DAC modes.

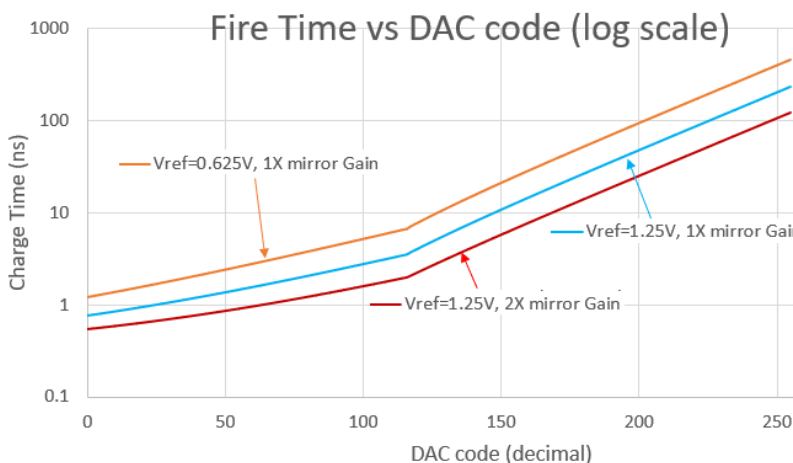


Figure 15: Fire Time Set by Clock Duty Cycle

I²C and Reg Map

Regmap

read/write backed by MTP	Register Bytes 0x10 to 0x16 can be read/written from/to and are loaded during start-up by 3 times programmable MTP memory.
read/write I2C only	These register Bytes can be read and written to/from via I2C but they are not associated with any nonvolatile memory addresses
read only	These bits are set internally by the SL2001 and can ONLY be read via I2C (not associated with any nonvolatile memory addresses)
read/reset status	The SL2001 will set bits of register 0x90 to one if an associated fault occurs. The user can reset any of these bits back to zero via I2C write (not associated with any nonvolatile memory addresses)
NVM action	Writing a one to bit one or zero of register 0x8A via I2C will cause the SL2001 to perform a write or read from the non volatile memory address in register 0x8B. After completing the requested action, the SL2001 will auto clear this bit back to a zero. (not associated with any nonvolatile memory addresses)

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0
Flux Time Control	0x10	FluxTime[7]	FluxTime[6]	FluxTime[5]	FluxTime[4]	FluxTime[3]	FluxTime[2]	FluxTime[1]	FluxTime[0]
Charge Time Cntrl	0x11	ChargeTime[7]	ChargeTime[6]	ChargeTime[5]	ChargeTime[4]	ChargeTime[3]	ChargeTime[2]	ChargeTime[1]	ChargeTime[0]
Fire Time Control	0x12	FireTime[7]	FireTime[6]	FireTime[5]	FireTime[4]	FireTime[3]	FireTime[2]	FireTime[1]	FireTime[0]
Function 3	0x13	SupplyOK_VTH[1]	SupplyOK_VTH[0]	VinOV_VTH[2]	VinOV_VTH[1]	VinOV_VTH[0]	DO NOT USE	VinUV_VTH[1]	VinUV_VTH[0]
Function 4	0x14	DutyCyleMode	FluxOV_VTH[1]	FluxOV_VTH[0]	FireOV_VTH[2]	FireOV_VTH[1]	FireOV_VTH[0]	FluxUV_VTH[1]	FluxUV_VTH[0]
Function 5	0x15	DigSoftRset	TChargeRef	TFireRef	TFluxRef[1]	TFluxRef[0]	TCharge2x	TFire2x	TFlux2x
Function 6	0x16	FluxOVBehavior[1]	FluxOVBehavior[0]	CresUVBehavior	FireUV_VTH[1]	FireUV_VTH[0]	DontSkip1stFlux	i2c_address[1]	i2c_address[0]
nvm_ctrl	0x8A	vpp_mode	keep these 3 bits at 000			vpp_req	wr_en	wr	rd
nvm_addr	0x8B	nvm_addr[7:0]							
nvm_wdata	0x8C	nvm_wdata[7:0]							
nvm_rdata	0x8D	nvm_rdata[7:0]							
status_fault	0x90	Over Temp	VinOV	VinUV	CresUV pre-Charge	CresOV pre Charge	CresOV post Charge	CresUV post Charge	SupplyOK Fault

Table 3: Register Map

Non Volatile Memory (NVM)

In addition to real time I²C programmability during operation, registers 0x10 through 0x16 above can also be set via SL2001's three-time programmable Multiple Time Programmable (MTP) ROM, which will be loaded to those registers when the part starts-up. SL2001 also contains 219 additional One Time Programmable (OTP) Bytes in memory addresses (0x17-0x5F and 0x67-0xAF and 0xB7- 0xFF) that users can use as they wish. There are additional Bytes of memory that have no direct impact on product operation and can be loaded with any information, for example board or laser specific information that a microcontroller could use to modify register settings during operation due to temperature or other variations.

One example for use of the 219 Bytes of OTP would be to store board specific information about the optimal Flux Time Control (Register 0x10) codes for various laser temperatures and/or other environmental variants in order to achieve one or several desired Light power profiles. During operation, the temperature could then be sensed near to the laser, and the code could then be read back via I²C for the memory address associated with that temperature, such that the code in that memory address could then be written via I²C to register 0x10.

Protection and Fault information

The SL2001 offers several highly programmable fault options and settings. A brief summary of the Fault Options is shown below with more specific information regarding each option in the subsections below in *Table 4*.

Hiccup Mode (Default): When a Fault is registered in the Digital circuitry, the SL2001 will stop immediately and set both the **FluxOUT** and **FireOUT** pins to low (zero V) for 28ms. After 28ms, the SL2001 will check whether the fault is still present. If the fault is still present, the SL2001 will continue holding both **FluxOUT** and **FireOUT** low and wait another 28ms before checking the fault status again. Once the fault is no longer present (checking every 28ms), the SL2001 will immediately begin driving both the **FluxOUT** and **FireOUT** pins again per the previous clock and timing settings.

Mask Faults: The SL2001 can be programmed via One Time Programmable ROM or via I²C to not shutdown or react to any of the faults desired.

Fault Latch Off mode: The SL2001 can be programmed via One Time Programmable ROM or via I²C to not "hiccup" but rather to "latch off" when any of the selected faults are registered. If the SL2001 does latch-off due to a fault, then the **FluxOUT** and **FireOUT** pins will be held low until either 1 of the 2 events occurs:

The DigSoftReset bit (bit 7 of register 0X15) is set to a 1 via the I²C interface (this bit will be reset back to 0 automatically upon reset)

The **AV_{dd}** voltage is brought below 1V, then brought back up above 3V

Upon either event 1 or 2 occurring, the SL2001 registers will go through its start-up sequence such that all registers will be set according to the NVM settings and then check whether any faults exist before beginning to drive the **FluxOUT** and **FireOUT** pins again.

Fault Condition	Action
V _{DD} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault Bit (Register 0x90 bit 0)
Cres Low After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit1)
Cres High After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit2)
Cres High Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit3)
Cres Low Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit4)
V _{in} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit5)
V _{in} High	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit6)
Over Temperature	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit7)

Table 4: Fault Conditions

Fault Behavior During Device Start-up

During start-up, approximately 100us after **AV_{dd}** has reached a voltage of ~2.5V, SL2001 will clear the reset for the internal Digital Engine. **AV_{dd}** supply protection then activates. If at the time the Digital Engine clears reset, **AV_{dd}** is still lower than 4.5V, a fault flag will be asserted to the Fault Register. During this initialization period the IC will not enter hiccup mode and waits for this fault to be cleared. Once **AV_{dd}** is above the target SupplyOK Fault rising threshold, the startup sequence will be completed, and functional mode will be enabled.

To avoid getting a SupplyOK fault flag in fault status register, the **AV_{dd}** slew rate needs to be fast enough so that after **AV_{dd}** cross 2.5V, within 100us, **AV_{dd}** will reach 4.5V. Slew rate can be set by the equation below:

$$\text{Equation 9 : } AV_{dd} \text{ Slew rate} > (4.5V - 2.5V)/100us = 2V/100us$$

Reading data from the OTP will take approximately 50us after the internal Digital Engine clears the reset state. The **V_{in}** Over Voltage and Under Voltage protection will be enabled with corresponding NVM pre-programmed thresholds. If a **V_{in}** UV or **V_{in}** OV fault exists when OTP read is complete, the corresponding fault bit will be asserted (*Table 3*). If the reported Fault is enabled, SL2001 will enter the shutdown mode with the corresponding pre-programmed shutdown state (Hiccup Mode or Latched Off).

In order to avoid the extra delay time during start up caused by a **V_{in}** UV Fault please note the following:

- 1) Ramp up the **V_{IN}** supply to the target voltage before the **AV_{dd}** supply ramp or Use the same supply for both **V_{IN}** and **AV_{dd}** (Set Vin UV threshold to be lower than 5V on the rising edge).
- 2) Ramp up **V_{IN}** and **AV_{dd}** at the same time while keeping the **V_{IN}** supply slew rate higher than the equation below:

$$\text{Equation 10: } V_{IN} > UV_{\text{thresholdRising}} / (3V / \text{SlewRate}_{AV_{dd}} + 150\mu s + T_{\text{dlyprogramable}})$$

The **CresSNS.UV_Precharge** comparator (see *Figure 18*) is active after OTP read is completed to detect a short circuit from the cathode of the laser to ground. The **V_{in}** voltage should not rise higher than the laser light threshold until at least 200us after the **AV_{dd}** voltage is higher than 2.5V for this start-up short detection to trip immediately during start-up (before the laser light causes an eye safety concern).

After all data from the OTP has been read, the device will wait a programmable amount of time (Tdlyprogrammable) before the **FluxOUT** and **FireOUT** signals are enabled (allowed to go high), according to [Table 5](#).

Waveforms for different startup examples are available in the section *Startup Fault Condition Examples*

bit5	bit4	Register 0x00, bits 5:4, FuseTime
0	0	Delay time from OTP read complete to Function mode allow is 18us
0	1	Delay time from OTP read complete to Function mode allow is 89us
1	0	Delay time from OTP read complete to Function mode allow is 355us
1	1	Delay time from OTP read complete to Function mode allow is 888us

Table 5: Programmable delays for OTP read mode to full Function mode.

Figure 16 below shows the start-up waveforms for OTPrady, FunctionMode and the CresSNS Valid signal

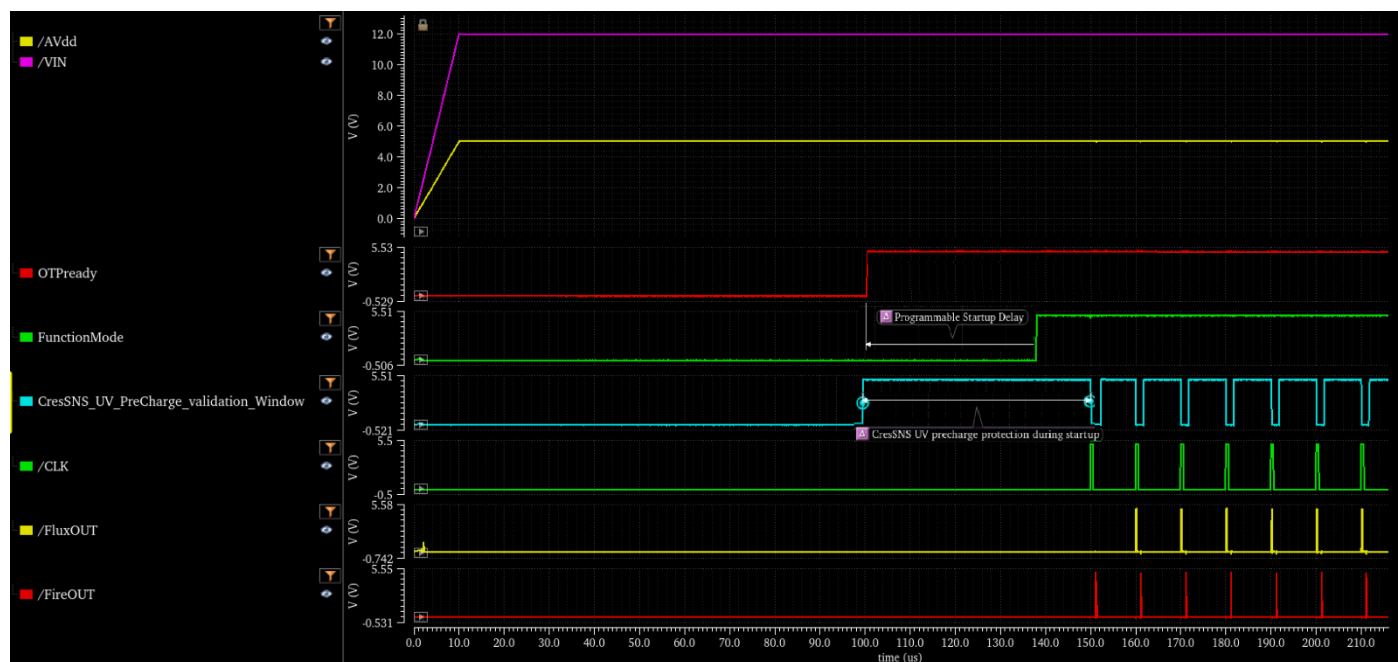


Figure 16: Startup Waveforms

During normal operation, the part reaction to a fault can be programmed. Register 0x01 (Fault Enable) individually sets each Fault such that it will cause an action, like the part shutting down. If the Fault Enable bit is not set (value of 0) for any individual fault and that fault type occurs, then the fault will be registered as a 1 in the status_fault register (0x90)

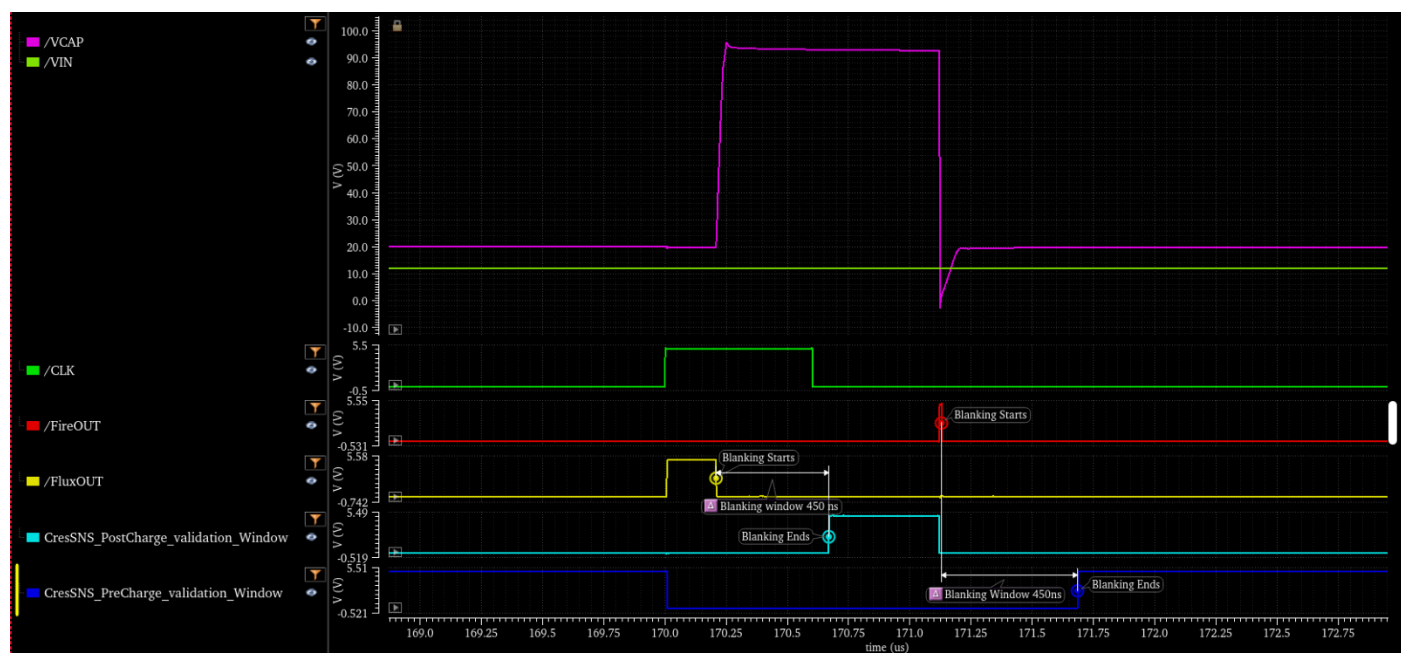


Figure 17: Fluxing and Firing Timing

Vin UV and OV Faults

The Table below shows the Fault Threshold Options for Vin Undervoltage and Overvoltage Faults. If the Vin UV fault is disabled, the SL2001 will continue to operate even with Vin at zero. The undervoltage Faults are still Monitored to give an indication of Vin falling below the intended supply voltage range. The SL2001 Vin pin is rated for operation up to 24V; however, lower overvoltage threshold options are available for the user to get an indication of Vin going above their intended supply voltage range.

Vin UV Voltage Options	Register 0x13	
	Bit 1	Bit 0
2.5V	0	0
4V	0	1
9.1V	1	0
11V	1	1

Table 6: Vin UV Options

Vin OV Voltage Options	Register 0x13		
	Bit 5	Bit 4	Bit 3
30V	0	0	0
27V	0	0	1
17.5V	0	1	0
15.5V	0	1	1
13.5V	1	0	0
7.5V	1	0	1
6.5V	1	1	0
5.5V	1	1	1

Table 7: Vin OV options

Cres Related Faults

The Cres_SNS pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in [Figure 18](#). Value options include 6.2M Ω or 6.8M Ω , with the fault threshold voltages varying per [Table 7: Vin OV options](#). Please ensure that the external resistor can support the maximum voltage that will be seen on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2001 takes when a fault as detected is described in [Table 5: Programmable delays for OTP read mode to full Function mode](#).

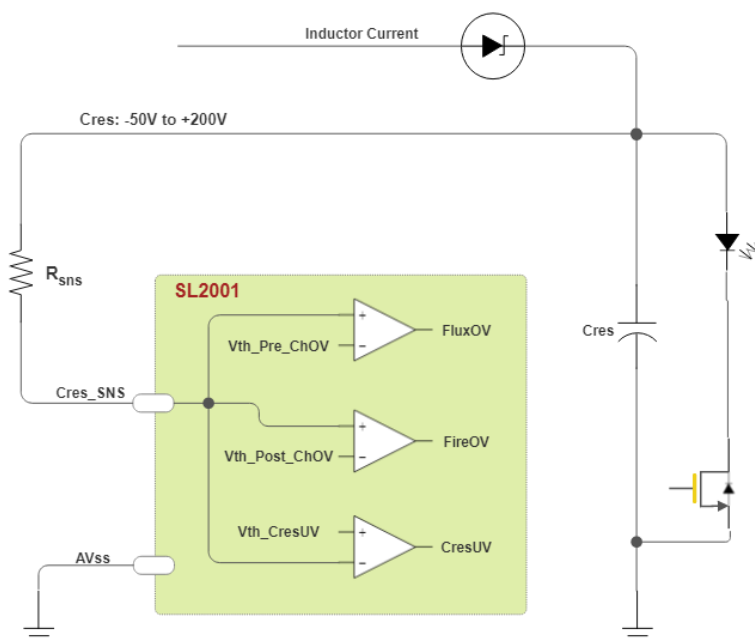


Figure 18: SL2001 Fault Diagram

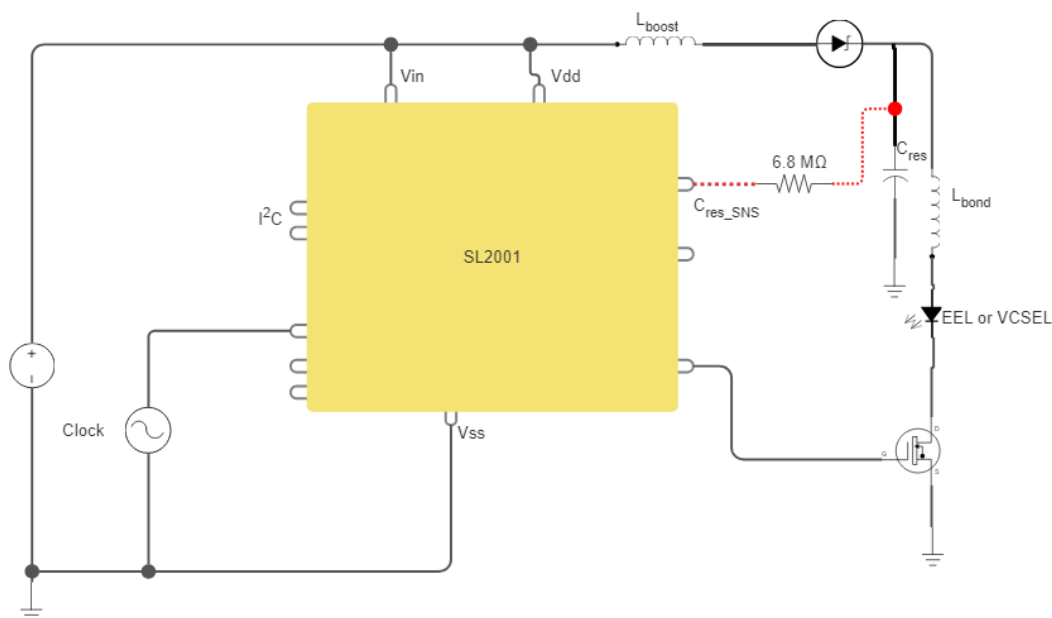


Figure 19: Cres Sense from the Anode Side

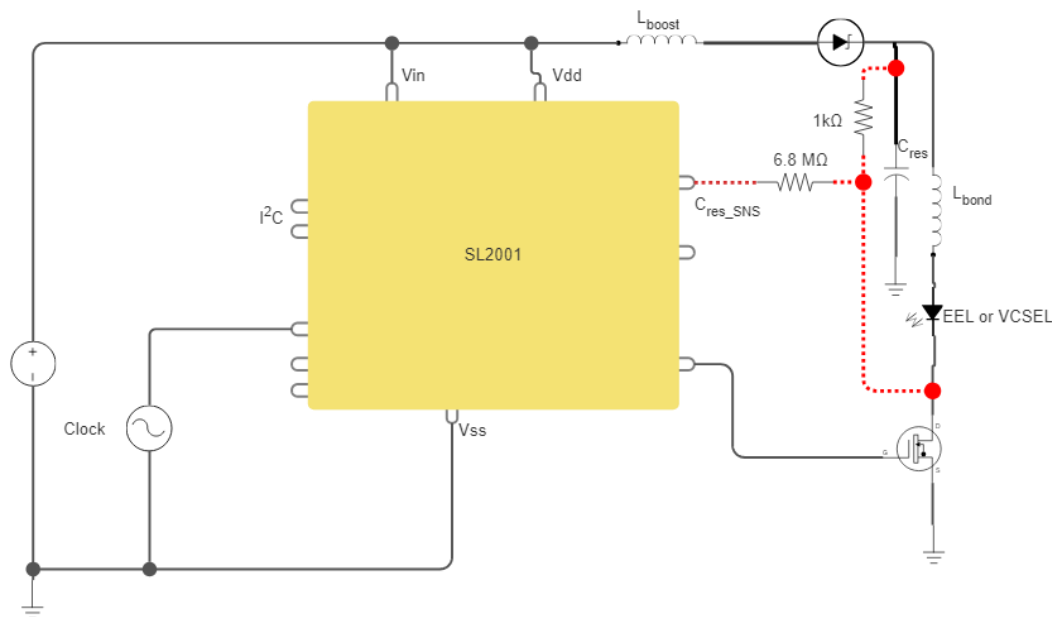


Figure 20: Cres Sense from the Cathode

It is also possible to sense at the Laser cathode as per [Figure 20](#). In an application where short detection of Laser Firing GaN FET is critical, using a cathode sensing scheme will ensure a more accurate short circuit detection.

For example, in [Figure 19](#), when a weak short circuit occurs across the Laser firing GaN FET, it might only produce 100mA of current going through the Schottky diode. Therefore, the voltage drop across the Schottky diode isn't significant enough to be detected as a Cres UV pre-charge fault. This can cause the Laser diode to continue to emit light without being properly controlled. The Laser cathode sensing scheme ensures more accurate short circuit detection because of the additional voltage drop across the laser diode. It is recommended to add a resistor across the laser diode, 1K ohm as shown in [Figure 20](#). This enables the Laser cathode to settle faster and sync with the anode after the laser firing event, see [Figure 21](#). Here an example waveform is shown without any resistor between Laser Anode and Cathode. In this case the Cathode voltage doesn't reflect the true Anode (VCAP node) voltage before or after Laser fired. The resistor value should be chosen based on the value of parasitic capacitance in the Laser firing path (including Laser Firing GaN Cds and PCB parasitic), so that the $5 \cdot RC$ time constant to be $< 320\text{ns}$. This ensures that the CresSNS input signal settles before the internal blanking time (for noise filtering) expires. When using 1K ohm RES across the laser, See [Figure 22](#), the Cathode voltage level will settle to the Anode voltage value after the RC delay time both before and after a Laser firing event.

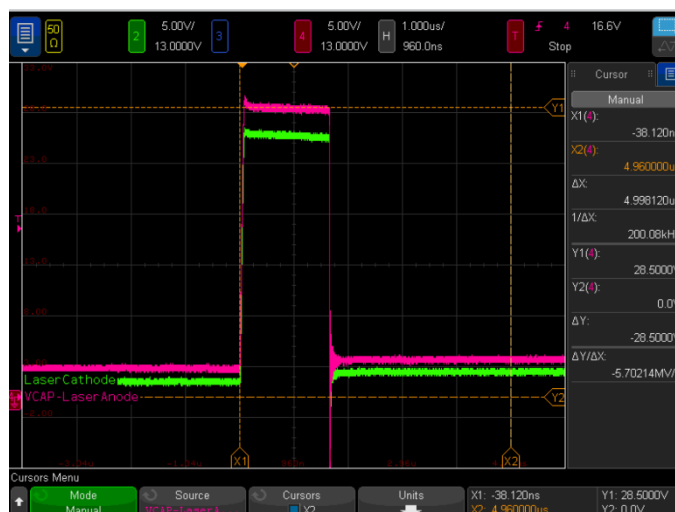


Figure 21: Laser Anode vs. Cathode without any resistor across Laser during operation

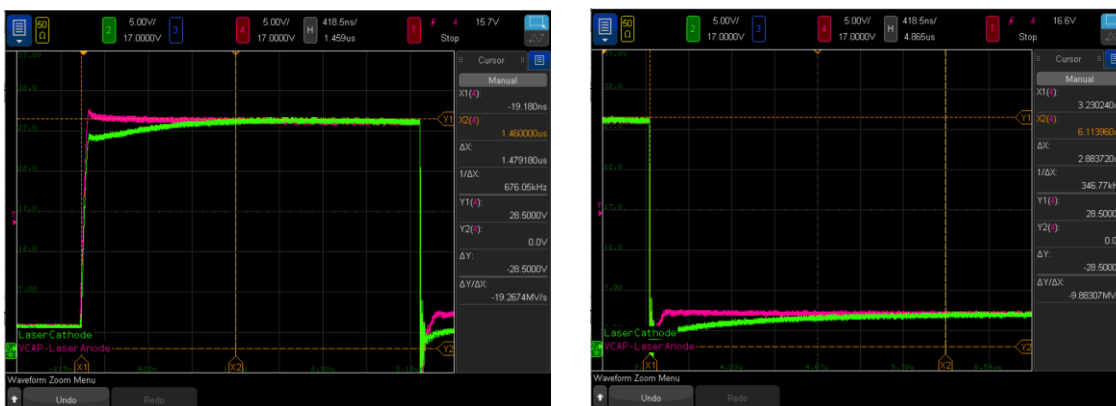


Figure 22: Laser Anode vs. Cathode with 1K ohm RES across Laser during operation

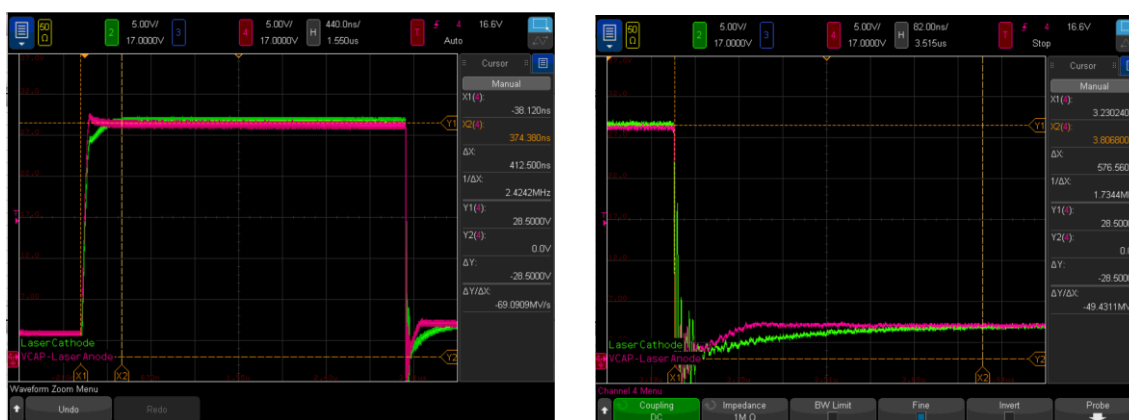


Figure 23: Laser Anode vs. Cathode with 180 ohm RES across Laser during operation

During the IC startup sequence, if V_{DD} and V_{IN} are biased separately and V_{DD} reaches 4.5V before V_{IN} , the SL2001 IC will be able to capture the short circuit between Laser firing GaN FET source and drain. The reaction to this fault condition, IC can be programmed to force the SL2001 to turn on the Fluxing GaN FET which directs current from V_{IN} to ground instead of going through the laser preventing laser from emitting light until SL2001 IC goes through a power cycle or is digitally reset via I²C. Figure 24 gives an example waveform using this cathode sensing scheme. In this example, the system starts up and encounters a short circuit between the Laser cathode and ground (source and drain of the Laser firing GaN FET). This protection scheme is only available when V_{IN} is above 4.5V to ensure accuracy and prevent mis-tripping. When the V_{IN} supply is ramping up, Laser diode will start to conduct current via the short circuit. Once the V_{IN} is above 4.5V, the short circuit is detected, and protection is activated. The FluxOUT pin will be latched to a high state to steer the current away from Laser to ground path.

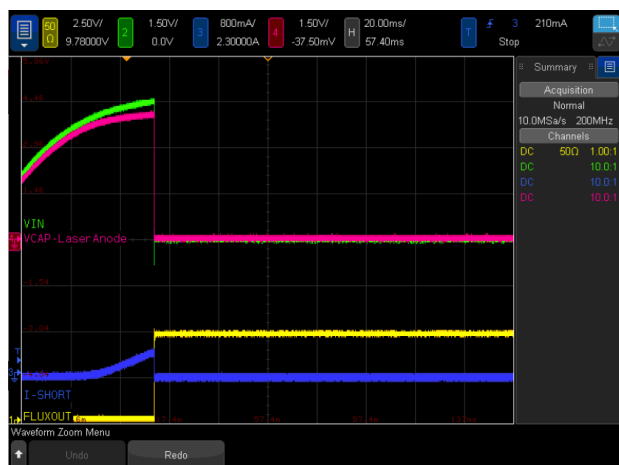


Figure 24: Laser firing GaN Short protection engaged after V_{DD} bias in place and during V_{IN} ramping up (cathode sense)

In applications where V_{DD} and V_{IN} supplies are combined the short circuit protection can still be triggered. However, because V_{DD} and V_{IN} are sharing the same supply, the Fluxing GaN will deplete V_{DD} and cause IC to go into power on reset and turn off the Flux GaN FET. If V_{IN} and V_{DD} try to rise again, a repeat of these events will occur if the short is still present. An input power fuse is recommended, to protect the system.

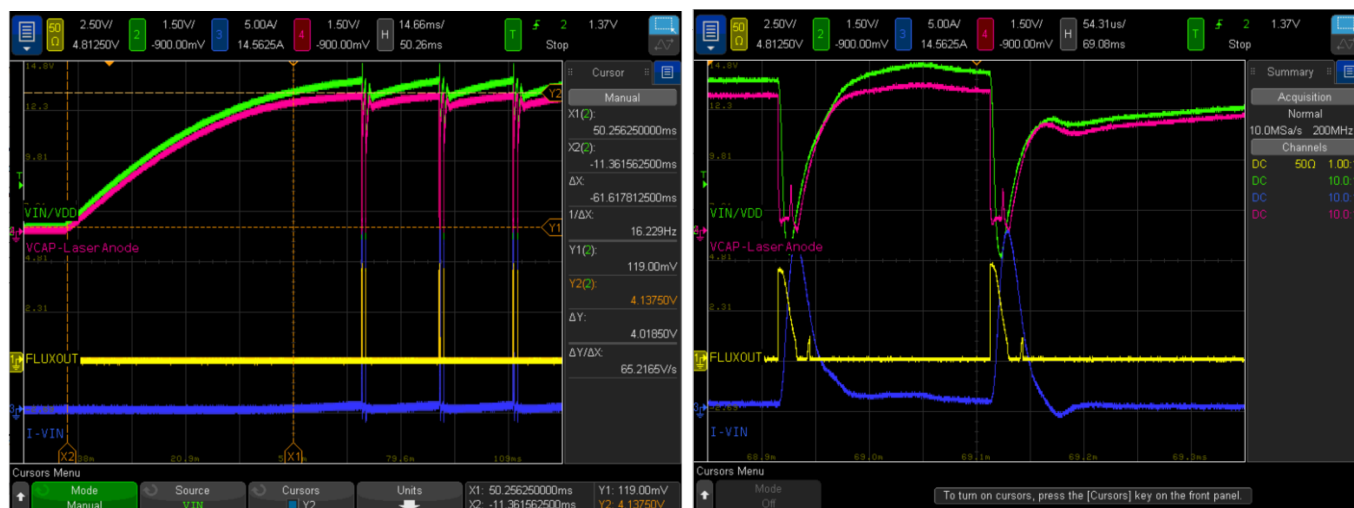


Figure 25: Laser firing GaN Short protection engaged when V_{IN} & V_{DD} are biased from the same supply and zoom in view (cathode sense)

During normal operation, a short circuit between the Laser cathode and ground can also be detected by the IC. An example of this occurrence is depicted in **Error! Reference source not found.** This short circuit occurs with a 1KHz repetition rate and is sensed using the laser cathode sensing scheme.



Figure 26: Laser firing GaN Short Circuit Protection engaged during operation when V_{IN} & V_{DD} are biased separately and zoom in view

Function	Cres Post Charge UV		Cres Post Charge OV		Cres Pre Charge UV		Cres Pre Charge OV	
Register	0x14, bits 4:2		0x16, bits 4:3		0x14, bits 1:0		0x14, bits 6:5	
Rsns value	6.2M Ω	6.8M Ω	6.2M Ω	6.8M Ω	6.2M Ω	6.8M Ω	6.2M Ω	6.8M Ω
code 0	5.5V	6V	59V	65V	Vin	Vin	18V	20V
code1	7.25V	8V	100V	110V	Vin – 1.5V	Vin – 1V	36V	40V
code2	8.15V	9V	146V	160V	Vin – 2V	Vin – 1.3V	54.4V	60V
code3	9.1V	10V	178V	195V	Vin – 3V	Vin – 2.3V	73V	80V
code4	10.9V	12V						
code5	12.7V	14V						
code6	16.3V	18V						
code7	20.85V	23V						

Table 8: SL2001 Fault Trigger Level Settings for Cres Voltage

Startup Fault Condition Examples

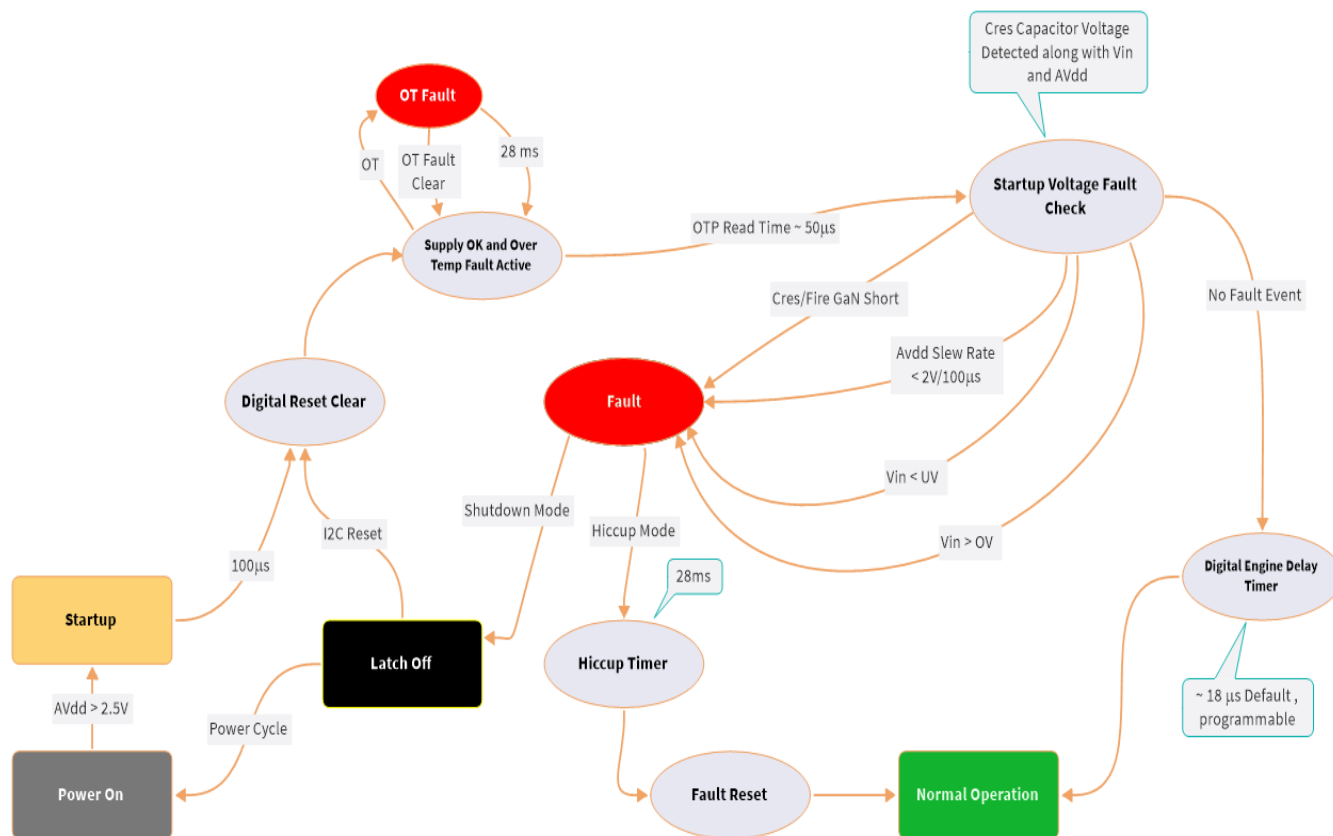
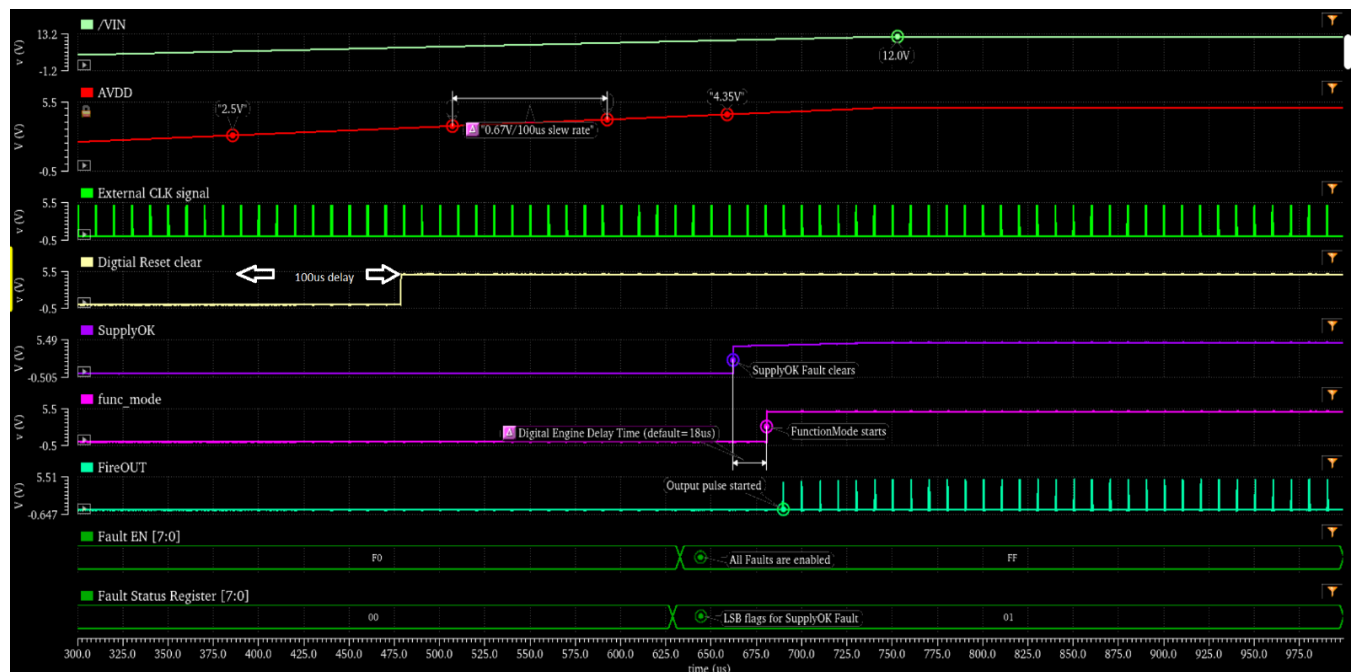


Figure 27: Basic Startup Sequence

Condition 1: **AV_{dd} slew rate < 2V/100us**

SupplyOK Fault = True When AV_{dd} slew rate is slower than 2V/100us, the start-up completes with SupplyOK Fault asserted.

The Startup sequence completion is gated by a SupplyOk Fault. As AV_{dd} rises above the Supply Fault clear threshold,



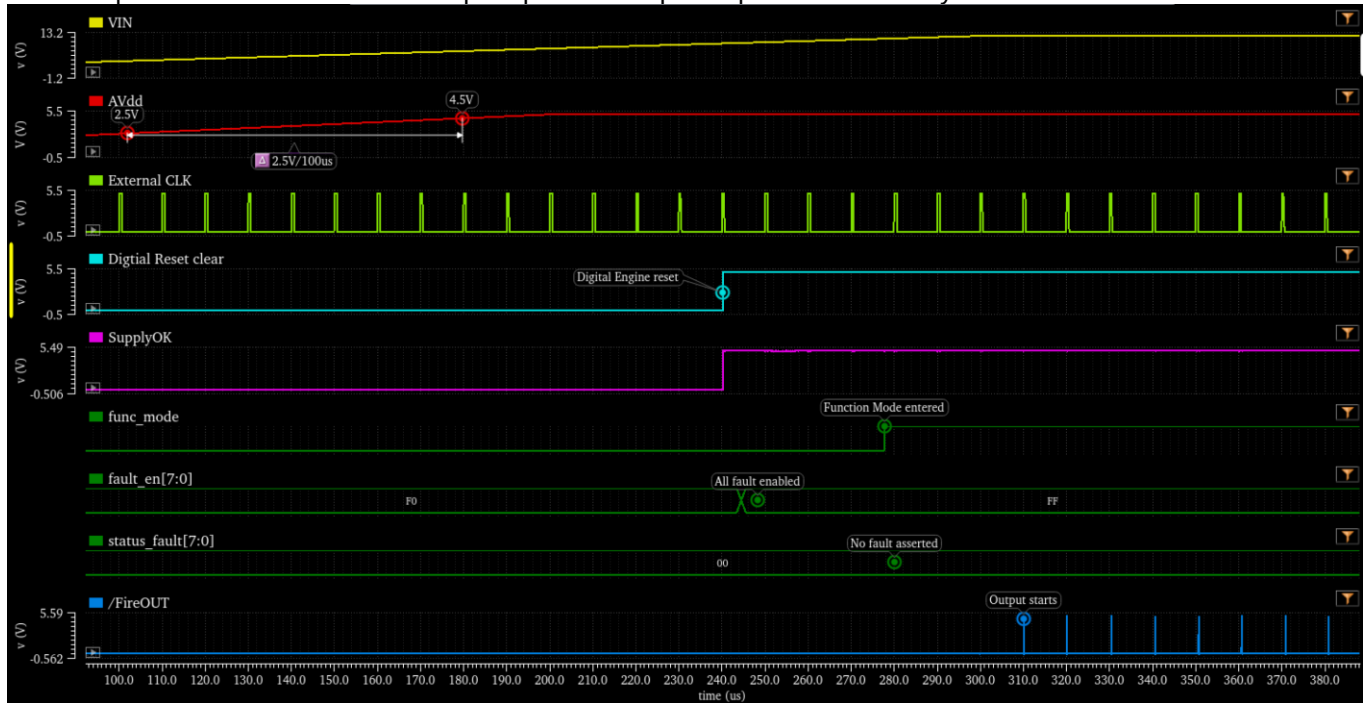
18us (the programable delay time) after, normal operation starts.

Condition 2:

AV_{dd} slew rate > 2V/100us

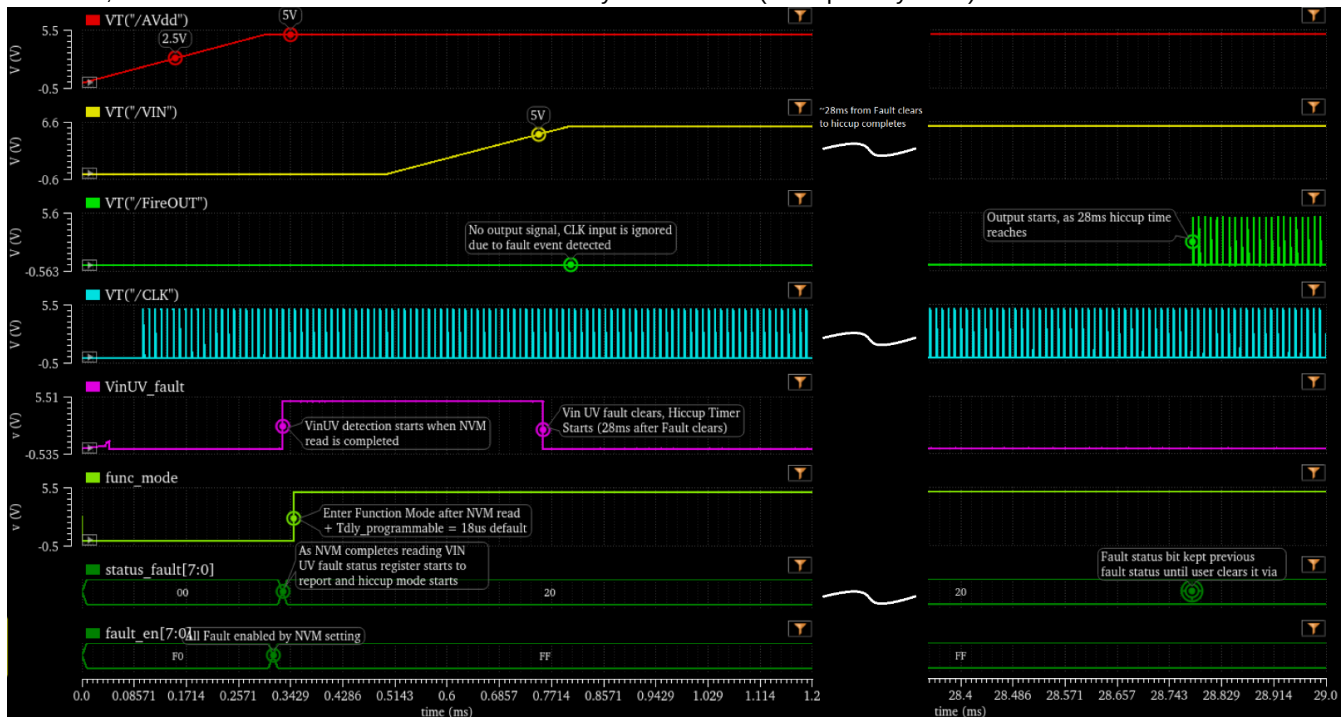
SupplyOK Fault = False

When the AV_{dd} slew rate is higher than 2V/100us, the start-up completes without a SupplyOK Fault being asserted. Normal operation starts after the startup sequence completes plus 18us of delay time.



Condition 3:

$AV_{dd} = 5V$ before V_{in} starts ramping: V_{in} UV Fault = True, Startup Mode = Hiccup. The AV_{dd} supply ramps up first and reaches 5V before the V_{in} supply starts. A V_{in} UV fault is reported and Hiccup Mode starts. After V_{in} reaches the V_{in} UV clear threshold, the IC enters normal function Mode. The delay will be 28ms (Hiccup Delay Time).

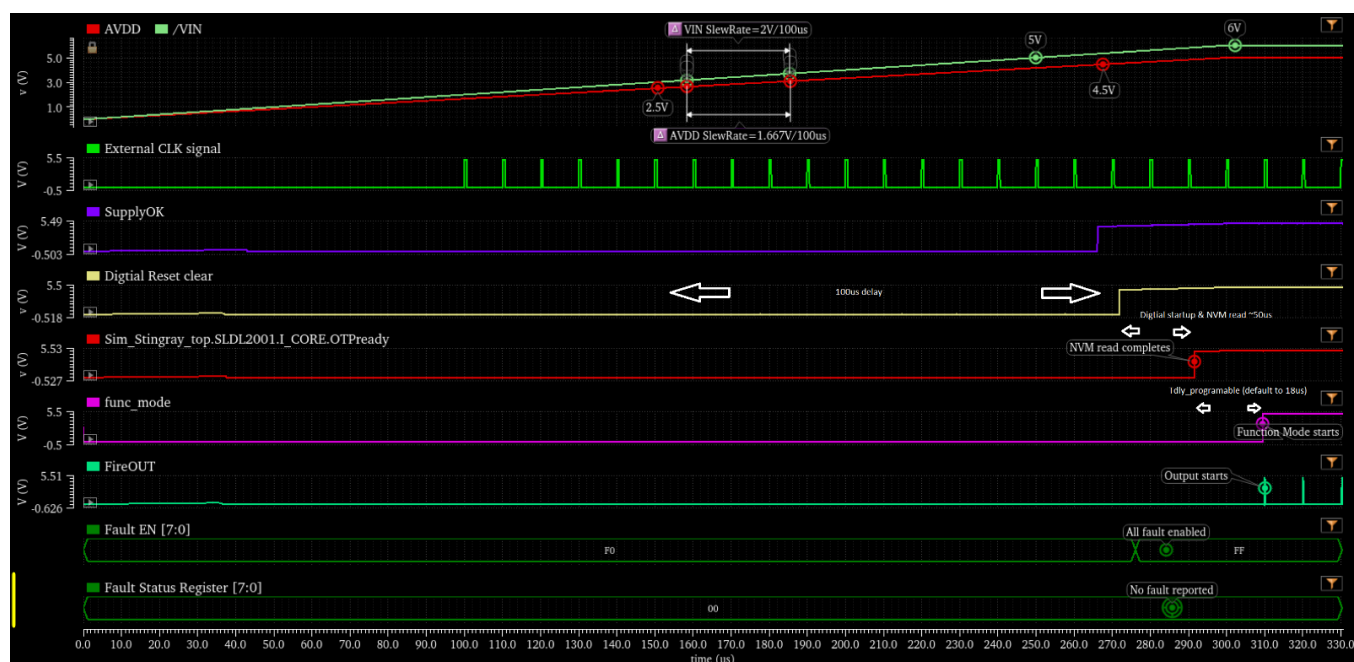


Condition 4: **$AV_{dd} = V_{IN} = 5V$;** **V_{in} UV thresholds set $< 5V$** **Fault Status = None**

AV_{dd} and V_{in} are connected to one supply (V_{in} UV threshold is pre-programmed to lower than 5V for the rising edge). No Fault is reported during startup. The Output starts as soon as the device normal functioning starts.

**Condition 5:** **V_{IN} slew rate = $2V/100\mu s$** **AV_{dd} slew rate = $1.667V/100\mu s$** **Fault Status = None**

AV_{dd} and V_{IN} ramp together while the V_{in} slew rate is $2V/100\mu s$ and the AV_{dd} Slew Rate $> 1.43V/100\mu s$



$= V / (3V / (1.667V / 100\mu s) + 150\mu s + 18\mu s)$ (see **Error! Reference source not found.**). This will avoid tripping the V_{in}
 $V_{thresholdRising} = 5V$ when entering Functional mode.

Reference Design

A reference design of an evaluation board using SL2001 is shown below.

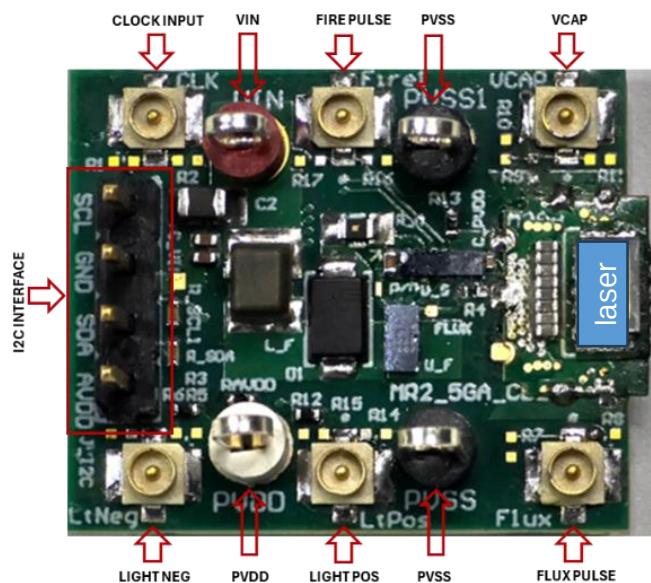
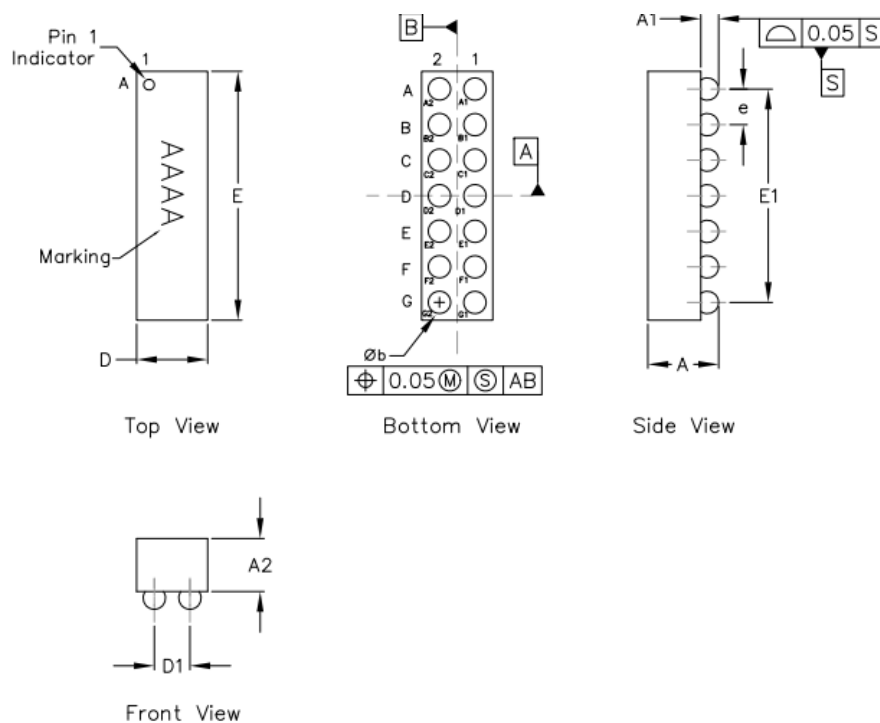


Figure 28: SL2001 Evaluation Board

Package Dimensions



COMMON DIMENSION	
SYMBOL	VALUE
A	0.995 ±0.05
A1	0.250 ±0.03
A2	0.745 REF
b	ø 0.315 ±0.03
D	1.000 ±0.025
E	3.500 ±0.025
D1	0.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC

NOTE:

1. TERMINAL PITCH IS DEFINE BY THE TERMINAL CENTER TO CENTER.
2. OUTER DIMENSION IS DEFINED BY CENTER LINES BETWEEN SCRIBE LINES
3. ALL DIMENSIONS IN MILLIMETER
4. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY
5. TOLERANCE IS ±0.02 UNLESS SPECIFIED OTHERWISE

Product Ordering Information

Part Number	Package	Feature	Shipping Method
SL2001-00	14 Pin bumped flip chip		

Note:

1)

Figure 29

Revision History

Revision	Date	Author	Note
1.0	3/25/2024	KB	Initial Release

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4795 Eastgate Mall, Suite 100, San Diego, CA 92121
Toll Free: (888) 637-3564 | Fax: (858) 373-0437 | www.powerdensity.com